CS146: Computer Architecture
Fall 2019
Homework #3
Due October 18, 2019 (Friday)

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1. **Register Renaming**

   (a) Write a piece of code (with a RISC ISA) that would make use of the renaming registers to avoid stalls, but would stall on a machine without renaming registers.

   (b) Now write a piece of code whose performance is limited by having too few renaming registers. Assume only 8 rename registers exist.

2. **Speculative Execution**

H&P Problem 3.22 (Page 297)

For this problem, make reasonable assumptions about latencies and the size of the ROB . For example, you can assume a 3 entry ROB to solve part a).

For part b) think of a simple extension to the basic scheme from section 3.7 – you do not need to do anything too complex (physical register files, etc).

3. **Static Scheduling and Loop Unrolling**

H&P Problem 4.8

4. **Software Pipelining**

H&P Problem 4.11