CS146: Computer Architecture
Fall 2019
Homework #5
Due November 15, 2019

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1. **Cache and TLB Design**

Consider a memory system with the following parameters:

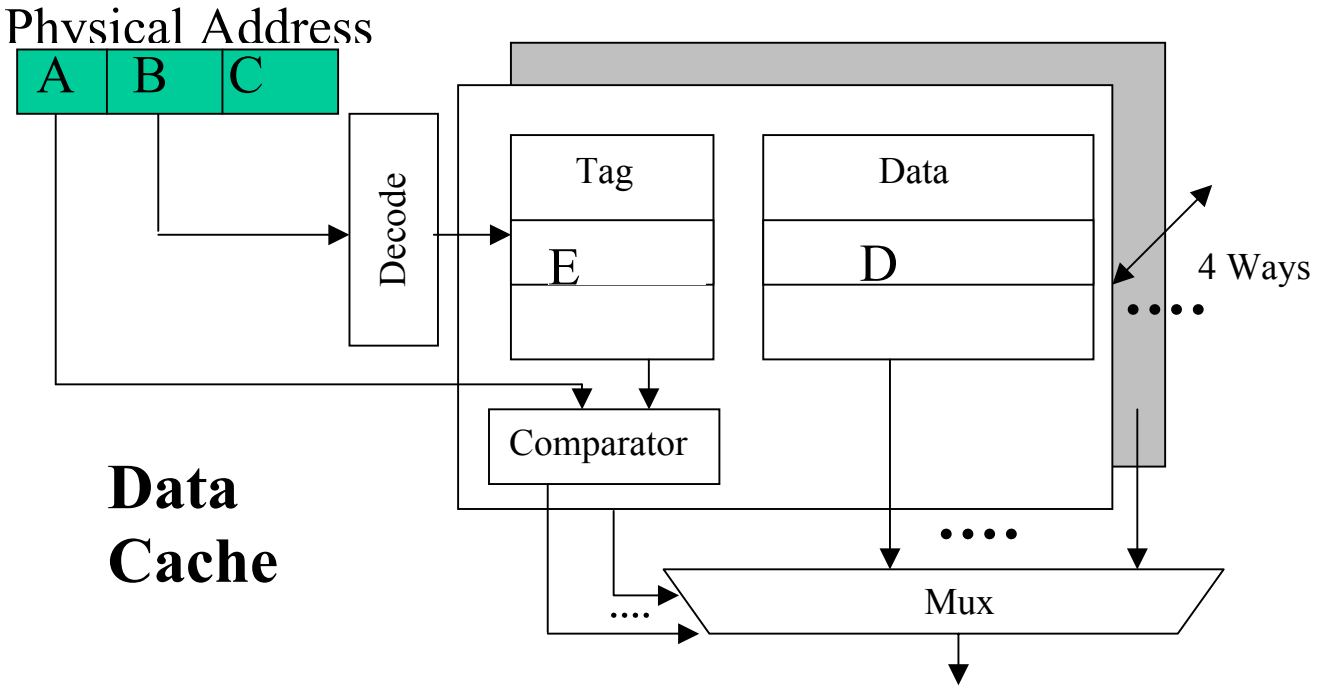
Translation Lookaside Buffer
- A total of 512 entries, organized as 4-way set associative
- LRU Replacement

L1 Cache
- 128KB, 4-way set associative, 32byte lines
- LRU replacement

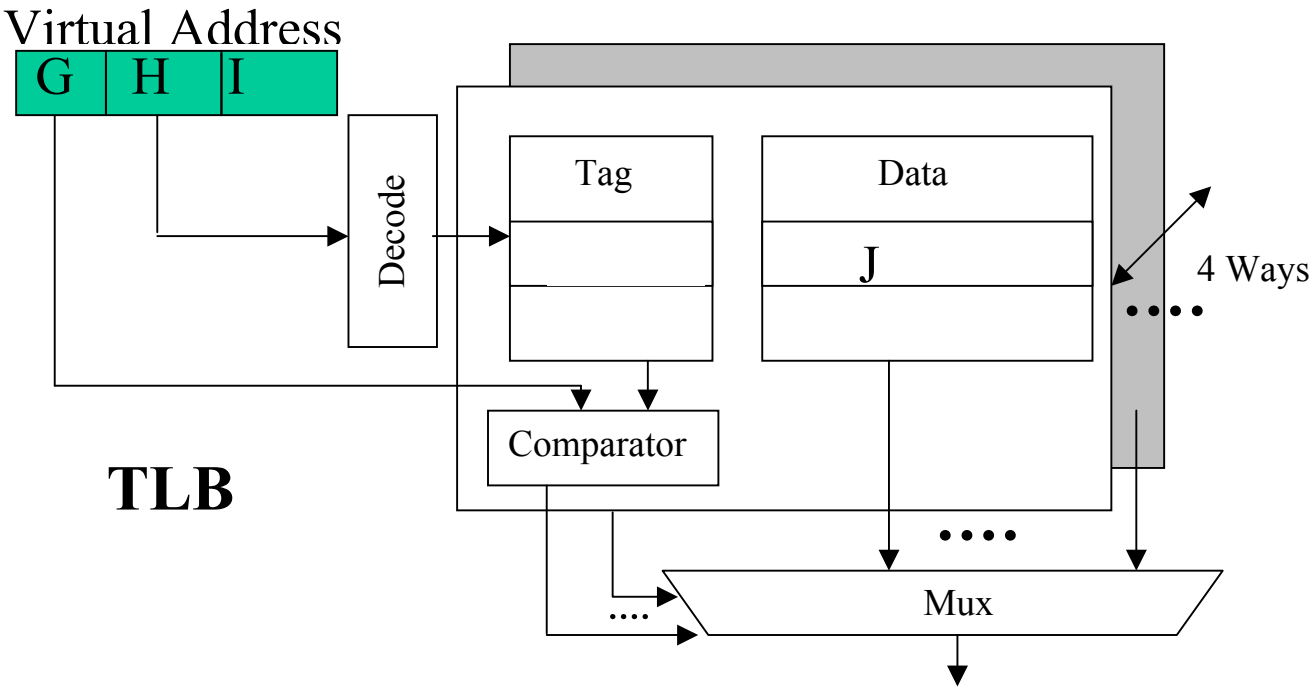
Memory
- 4GB Virtual Address Space
- 512MB of physical memory
- 4KB Page Size

The following page shows a labeled diagram of the cache and TLB. Please fill in the appropriate information in the boxes below.

L1 Cache		TLB	
A=	bits	G=	bits
B=	bits	H=	bits
C=	bits	I=	bits
D=	bits	J=	bits
E=	bits		



Data Cache



TLB

2. 3-Stage Coherence Protocol

Consider a bus-based, shared address-based multiprocessor in which each processor has a single level of data caching: the cache is 16KB total with 64-byte lines. It is direct-mapped. Assume an ownership-based, invalidation-based cache coherence protocol (i.e. the one we discussed in class and in Figure 6.12 of the textbook. Assume two processors on the bus. Write a sequence of read and write operations (using real address numbers) for these two processors that exercise all of the possible state transitions. In your solution clearly draw the relevant cache state diagrams and label all transitions with the same numbers you use to in your read/write sequences.

3. Coherence Protocol Design

Add a clean exclusive state (a state where the block is being read *only* by the local processor) to the basic snooping cache coherence protocol (Figure 6.12 on page 559). Assume that the cache can distinguish a read miss that will retrieve a block destined to have a private state (non-shared) from a read miss delivering a shared block. In other words, instead of just having Read Hit/Read Miss you will now have Read Hit/Read Miss Exclusive, and Read Miss Shared transition events. Show the protocol in the format of Figure 6.12 *and* describe all of the necessary changes made to the basic protocol in words.