Course Syllabus

Spring 2018: TTh 11:30-1:00PM in MD 221

This course provides an introduction to the design and analysis of digital CMOS VLSI circuits and systems. We begin by thinking about what constitutes a VLSI system and how to go about designing one—from physical layers that define the transistors and wires that comprise an integrated circuit to high-level understanding of assembling various building blocks. The course leverages switch-level abstraction of transistors to teach the design of static CMOS logic, but then delves into some details of transistor operation to understand circuit delays and power dissipation. We will see how to combine the basic logic elements to assemble more complex structures such as datapaths, memories, and control logic. The course introduces numerous industry-grade computer-aided design (CAD) tools used to facilitate the design, verification, and analysis of complex VLSI circuits and systems. The first half of the semester will focus on the basic mechanics of designing VLSI circuits. The second half of the semester will focus on a design project and discuss advanced topics such as low power design and variability.

Learning Outcomes:

1. Understand the fundamentals of IC technology components, scaling trends, and limitations.
2. Design VLSI circuits and systems utilizing modern IC design methodologies and design automation tools.
3. Analyze tradeoffs to optimize power, delay, and area.
4. Utilize modern CAD tools for IC design, simulation, verification, and automated logic synthesis and layout.
5. Explore circuit and higher-level solutions for low-power and variation-aware designs.
6. Anticipate future challenges in IC technologies and think critically about solutions.

Collaboration Statement:

Discussion and the exchange of ideas are essential to doing academic work. For assignments in this course, you are encouraged to consult with your classmates as you work on problem sets. However, after discussions with peers, make sure that you can work through the problem yourself and ensure that any answers you submit for evaluation are the result of your own efforts. List the names of students with whom you have collaborated on problem sets.

Instructor	Professor Gu-Yeon Wei Maxwell Dworkin 333 gywei@g.harvard.edu (mailto:guyeon@eecs.harvard.edu) Office hours: M 10-11AM, W 1-2PM, and by appointment (via email)

Teaching Fellow	Thomas (Hsea-Ching) Hsueh <hsuseh@seas.harvard.edu>
Lectures	TTh 11:30-1 PM in MD 221
Course Material	Lecture notes, handouts, assignments, etc. will be available on the course canvas site.
Text	*CMOS VLSI Design: a Circuits and Systems Perspective*, 4th ed., by Weste and Harris
Prerequisites	ES50 or Physics 15b, CS141 or permission of instructor. Basic understanding of circuits, digital logic, and programming will be useful. ES154 is also a plus, but not required.
Assignments	Weekly handwritten problem sets and periodic CAD-based exercises. No late submissions accepted except extraordinary circumstances.
Final Project	Datapath design and validation for a deep neural network accelerator, part of a system-on-chip for machine learning.
Exams	In-class 90 min midterm: **March 8, 2018 at 11:30-1PM** Comprehensive final exam: **Sat, May 12 2-5PM**
Grading	*Approximate* breakdown of percentages used to calculate final grades: Midterm Exam = 15% PSets & Labs = 30% Final Exam = 25% Final Project = 20% Other = 10% Please note % of grades in canvas does not necessarily reflect your actual grade. Final grades will be determined on a curve.

Tentative list of lecture topics

Lecture	Topic	Reading
1	Course intro and overview of VLSI design	W&H Ch 1
2	Transistors, RC models, delay	W&H Ch 1-4
3	CMOS logic	W&H Ch 1.4 & 9.1-2
4	Logical effort	W&H Ch 4.4-5
5	Wires	W&H Ch 6
6	IC technology and CAD tools	W&H Ch 3, 8
7	Latches, flip-flops, and clocking	W&H Ch 10
8	Adders and other datapath subsystems	W&H Ch 11
9	Memory and array subsystems	W&H Ch 12
10	Design methodologies	W&H Ch 14
11	Advanced memories and datapath circuits	W&H Ch 11, 12
12	Design for testability and manufacturability	W&H Ch 7, 15
13	Power, power delivery, and low-power design	W&H Ch 5, 9, 13
14	Fast logic and wires	W&H Ch 9, 13
15	IO, packaging, and special-purpose subsystems	W&H Ch 13
16	Technology scaling and future of VLSI	W&H Ch 7