CS148/CS248:
Design of VLSI Circuits and Systems

http://www.eecs.harvard.edu/cs148

Spring 2013: Tues/Thurs 11:30-1PM in MD323

This course provides an introduction to the design and analysis of digital CMOS VLSI circuits and systems. We begin by thinking about what constitutes a VLSI system and how to go about designing one—from physical layers that define the transistors and wires that comprise an integrated circuit to high-level understanding of assembling various building blocks. The course leverages switch-level abstraction of transistors to teach the design of static CMOS logic, but then delves into some details of transistor operation to understand circuit delays and power dissipation. We will see how to combine the basic logic elements to assemble more complex structures such as datapaths, memories, and control logic. The course introduces numerous industry-grade computer-aided design (CAD) tools used to facilitate the design, verification, and analysis of complex VLSI circuits and systems. The first half of the semester will focus on the basic mechanics of designing VLSI circuits. The second half of the semester will focus on a design project and discuss advanced topics such as low power design and variability.

Learning Outcomes

1. Understand the fundamental of IC technology components, scaling trends, and limitations.
2. Design VLSI circuits and systems utilizing modern IC design methodologies and design automation tools.
3. Analyze tradeoffs to optimize power, delay, and area.
4. Utilize modern CAD tools for IC design, simulation, verification, and automated logic synthesis and layout.
5. Explore circuit and higher-level solutions for low-power and variation-aware designs.
6. Anticipate future challenges in IC technologies and think critically about solutions.

Collaboration Statement

Discussion and the exchange of ideas are essential to doing academic work. For assignments in this course, you are encouraged to consult with your classmates as you work on problem sets. However, after discussions with peers, make sure that you can work through the problem yourself and ensure that any answers you submit for evaluation are the result of your own efforts. List the names of students with whom you have collaborated on problem sets.

Instructor	Prof. Gu-Yeon Wei MD 333 guyeon@eecs.harvard.edu Office hours TBD
TF	Mario Lok MD 311 mlok@seas.harvard.edu Office hours TBD
Lectures	Tues and Thurs, 11:30-1PM in MD323
Course Material	Lecture notes, handouts, assignments, etc. will all be available on the course web site
Text	**Highly recommended:** • *CMOS VLSI Design: a Circuits and Systems Perspective*, 4th ed. by Weste and Harris **Useful:** • *Digital Integrated Circuits: A Design Perspective* by Rabaey, Chandraksan and Nikolic • *Logical Effort: Designing Fast CMOS Circuits* by Sutherland, Sproull and Harris • *Skew-tolerant Circuit Design* by Harris. • *Device electronics for integrated circuits* by Muller and Kamins
Prerequisites	ES50 or Physics 15b, CS141 or permission of instructor. Basic understand- ing of circuits, digital logic, and programming will be useful. ES154 is also a plus, but not required.
Assignments	PSets, labs, project write-ups, etc. ordinarily due in class on Thursdays. A total of 3 late days allowed.
Design project	• CS148 students will have the option to design a simple processor or propose a small-scale custom VLSI design (by permission) • CS248 students *must* propose and design a custom VLSI subsystem
CS248	Additional paper reading, presentation, and discussions will be required for CS248 students. CS148 are welcome to attend, but are not required to present.
Exams	One in-class midterm exam and a 3-hr final exam
Grading	PSets: 20%; Design project: 20%; Midterm: 20%; Final: 25% Class participation: 15%

Tentative Course Calendar
(subject to change)

Date	Topic	Due
1/29	Course intro and overview of VLSI design	
1/31	Transistors, wires, and RC models	
2/5	Transistors, wires, and RC models (continued)	
2/7	Logic gates and RC delay	HW1
2/12	Logical effort	
2/14	Design methodologies, fabrication, and layout	HW2
2/19	Overview of CAD tools (schematic, layout, and simulations)	
2/21	Clocking, latches, and flip-flops	HW3
2/26	Adders and other DP blocks	
2/28	SRAMs	HW4
3/5	More on adders plus multipliers	
3/7	More on memories	HW5
3/12	Design methodologies + Design project overview	
3/14	**In-class midterm** (up to SRAMs)	Project Proposal (3/15 11:59PM)
3/19	*Spring break*	
3/21	*Spring break*	
3/26	Design for testability	
3/28	Power + power delivery	Project Part 1
4/2	Low-power design	
4/4	Fast logic (dynamic, skewed, etc.)	
4/9	Fast wires for communication and clocking	
4/11	Technology scaling and variations	Project Part 2
4/16	Design for manufacturability	

Date	Topic	Due
4/18	Variation-aware design	
4/23	Packaging	
4/25	Special circuits and subsystems	Project Part 3
4/30	Course review	
5/9	**Project completion** (end of reading period)	Project Report
TBD	**Final Exam**	