

David M. Brooks

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EDUCATION

- Princeton University.** Doctor of Philosophy in Electrical Engineering, 2001.
- Princeton University.** Master of Arts in Electrical Engineering, 1999.
- University of Southern California.** Bachelor of Science in Electrical Engineering, 1997.

ACADEMIC AND PROFESSIONAL EXPERIENCE

Gordon McKay Professor of Computer Science, School of Engineering and Applied Sciences, Harvard University (July 2009–Present).

John L. Loeb Associate Professor of the Natural Sciences, School of Engineering and Applied Sciences, Harvard University (July 2007–June 2009).

Associate Professor of Computer Science, School of Engineering and Applied Sciences, Harvard University (July 2006–June 2009).

- Areas of Interest: Computer Architecture, Embedded and High-Performance Computer System Design.
- Pursuing research in computer architectures and the hardware/software interface, particularly systems that are designed for technology constraints such as power dissipation, reliability, and design variability.

Assistant Professor of Computer Science, Division of Engineering and Applied Sciences, Harvard University (September 2002–July 2006).

Research Staff Member, IBM T.J. Watson Research Center, (September 2001–September 2002).

- Conducted analysis of the optimal power-performance pipeline depth of microprocessors.
- Developed IBM PowerTimer toolkit for architectural power-performance modeling.
- Assisted in concept phase and high-level design phase power-performance analysis for the Sony-Toshiba-IBM Cell Processor and the IBM POWER6 microprocessor.

Research Assistant, Princeton University, (July 1997–September 2001).

- Investigated the potential for dynamic thermal management in microprocessor designs.
- Developed the Wattch architectural power-modeling toolkit.
- Investigated the potential for narrow bitwidth optimizations for power-performance optimizations in ALUs and functional units.

Research Intern, IBM T.J. Watson Research Center, (June 2000–September 2000).

Research Intern, Intel Corporation, (June 1999–September 1999).

HONORS AND AWARDS

Papers selected for IEEE Micro's "Top Picks in Computer Architecture" special issue in 2005, 2007, and 2008.

Best Paper Award, International Symposium on High-Performance Computer Architecture, 2009.

DARPA/MTO Young Faculty Award, 2007.

1st Prize, Phase 2 of SRC SoC Design Challenge, October, 2006.

2nd Prize, Phase 1 of SRC SoC Design Challenge, October, 2005.

Best Paper Award, International Symposium on Microarchitecture, 2005.

National Science Foundation CAREER Award, February, 2005.

IBM Faculty Partnership Award, 2004–2005.

MICRO 2002 paper selected as one of the four Best IBM Research Papers in Computer Science, Electrical Engineering and Math published in 2002.

National Science Foundation Graduate Research Fellow, 1998-2001.

Princeton University Gordon Wu Graduate Fellow, 1997-2001.

University of Southern California Trustee Scholar, 1993-1997.

REFEREED CONFERENCE PUBLICATIONS

Meeta S. Gupta, Jude Rivers, Pradip Bose, Gu-Yeon Wei and David Brooks. "Tribeca: Design for PVT Variations with Local Recovery and Fine-grained Adaptation," *42nd International Symposium on Microarchitecture*, December, 2009.

Kristen Lovin, Benjamin Lee, Xiaoyao Liang, David Brooks, Gu-Yeon Wei. "Empirical Performance Models for 3T1D Memories," *27th International Conference on Computer Design*, October, 2009.

Xiaoyao Liang, Benjamin Lee, Gu-Yeon Wei and David Brooks. "Design and Test Strategies for Microarchitectural Post-fabrication Tuning," *27th International Conference on Computer Design*, October, 2009.

Mark Hempstead, Gu-Yeon Wei, and David Brooks. "An Accelerator-based Wireless Sensor Network Processor in 130nm CMOS," (Invited paper) *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES-09)*, October, 2009.

Michael Lyons and David Brooks. "The Design of a Bloom Filter Hardware Accelerator for Ultra Low Power Systems," *International Symposium on Low Power Electronics and Design*, August, 2009.

Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Software-Assisted Hardware Reliability: Abstracting Circuit-level Challenges to the Software Stack," *46th Design Automation Conference (DAC)*, July, 2009.

Krishna Rangan, Gu-Yeon Wei, and David Brooks. "Thread Motion: Fine-Grained Power Management for Multi-Core Systems," *36th International Symposium on Computer Architecture*, June, 2009.

Meeta S. Gupta, Vijay Janapa Reddi, Gu-Yeon Wei, and David Brooks. "An Event-Guided Approach to Handling Inductive Noise in Processors," *12th Design, Automation, and Test in Europe Conference*, April, 2009.

Kevin Brownell, A. Durlov Khan, David Brooks, Gu-Yeon Wei. "Place and Route Considerations for Voltage Interpolated Designs," *10th International Symposium on Quality Electronic Design (ISQED)*, March 2009.

Vijay Janapa Reddi, Meeta S. Gupta, Glenn Holloway, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Voltage Emergency Prediction: A Signature-Based Approach To Reducing Voltage Emergencies," *15th International Symposium on High-Performance Computer Architecture*, February, 2009. **Received Best Paper Award**

Benjamin C. Lee, Jamison Collins, Hong Wang, and David Brooks. "CPR: Composable Performance Regression for Scalable Multiprocessor Models," *41st International Symposium on Microarchitecture*, December, 2008. **Nominated for Best Paper Award**

Kevin Brownell, Gu-Yeon Wei and David Brooks. "Evaluation of Voltage Interpolation to Address Process Variations," *International Conference on Computer-Aided Design*, November, 2008.

Gu-Yeon Wei, David Brooks, A. Durlov Khan and Xiaoyao Liang. "Instruction-driven Clock Scheduling with Glitch Mitigation," *International Symposium on Low Power Electronics and Design*, August, 2008. **Nominated for Best Paper Award**

Xiaoyao Liang, Gu-Yeon Wei, and David Brooks. "ReVIVaL: Variation Tolerant Architecture Using Voltage Interpolation and Variable Latency," *35th International Symposium on Computer Architecture*, June, 2008. **Selected as one of the Top Picks in Computer Architecture in 2008.**

Mark Hempstead, Gu-Yeon Wei, and David Brooks. "System Design Considerations for Sensor Network Applications," *International Symposium on Circuits and Systems*, May, 2008.

Benjamin C. Lee and David Brooks. "Efficiency Trends and Limits from Comprehensive Microarchitectural Adaptivity," *International Conference on Architectural Support for Programming Languages and Operating Systems*, March, 2008.

Meeta S. Gupta, Krishna K. Rangan, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "DeCoR: A Delayed Commit and Rollback Mechanism for Handling Inductive Noise in Microprocessors," *14th International Symposium on High-Performance Computer Architecture*, February, 2008.

Benjamin C. Lee and David Brooks. "Roughness of Microarchitectural Design Topologies and its Implications for Optimization," *14th International Symposium on High-Performance Computer Architecture*, February, 2008.

Wonyoung Kim, Meeta Gupta, Gu-Yeon Wei, and David Brooks. "System Level Analysis of Fast, Per-Core DVFS using On-Chip Switching Regulators," *14th International Symposium on High-Performance Computer Architecture*, February, 2008.

Xiaoyao Liang, Gu-Yeon Wei, and David Brooks. "A Process-Variation-Tolerant Floating-Point Unit with Voltage Interpolation and Variable Latency," *IEEE International Solid-State Circuits Conference*, February, 2008.

Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, and David Brooks. "Process Variation Tolerant 3T1D-Based Cache Architectures," *40th International Symposium on Microarchitecture*, December, 2007. **Nominated for CACM special issue consideration by SIGMICRO. Selected as one of the Top Picks in Computer Architecture in 2007.**

Xiaoyao Liang, Kerem Turgay, and David Brooks. "Architectural Power Models for SRAM and CAM Structures Based on Hybrid Analytical/Empirical Techniques," *International Conference on Computer Aided-Design*, November, 2007.

Meeta S. Gupta, Krishna K. Rangan, Michael D. Smith, Gu-Yeon Wei, and David M. Brooks. "Towards a Software Approach to Mitigate Voltage Emergencies," *International Symposium on Low Power Electronics and Design*, August, 2007.

Meeta S. Gupta, Jarod L. Oatley, Russ Joseph, Gu-Yeon Wei, and David Brooks. "Understanding Voltage Variations in Chip Multiprocessors using a Distributed Power-Delivery Network," *10th Design, Automation, and Test in Europe Conference*, April, 2007.

Benjamin Lee, David Brooks, Bronis de Supinski, Martin Schulz, Karan Singh, and Sally McKee. "Methods of Inference and Learning for Performance Modeling of Parallel Applications," *Symposium on Principles and Practice of Parallel Programming*, March, 2007.

- Benjamin Lee and David Brooks. "Illustrative Design Space Studies with Microarchitectural Regression Models," *13th International Symposium on High-Performance Computer Architecture*, February, 2007.
- Xiaoyao Liang and David Brooks. "Mitigating the Impact of Process Variations on CPU Register File and Execution Units," *39th International Symposium on Microarchitecture*, December, 2006.
- Xiaoyao Liang and David Brooks. "Microarchitecture Parameter Selection to Optimize System Performance under Process Variation," *International Conference on Computer Aided-Design*, November, 2006.
- Benjamin Lee and David Brooks. "Accurate and Efficient Regression Modeling for Microarchitectural Performance and Power Prediction," *International Conference on Architectural Support for Programming Languages and Operating Systems*, October, 2006.
- Lukasz Strozek and David Brooks. "Efficient Architectures through Application Clustering and Architectural Heterogeneity," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October, 2006.
- Mark Hempstead, Gu-Yeon Wei, and David Brooks. "Architecture and Circuit Techniques for Low Throughput, Energy Constrained Systems Across Technology Generations," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October, 2006.
- Yingmin Li, Benjamin Lee, David Brooks, Zhigang Hu, Kevin Skadron. "Impact of Thermal Constraints on Multi-Core Architectures," *10th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems*, May, 2006.
- Yingmin Li, Benjamin Lee, David Brooks, Zhigang Hu, Kevin Skadron. "CMP Design Space Exploration Subject to Physical Constraints," *12th International Symposium on High-Performance Computer Architecture*, February, 2006.
- Qiang Wu, Vijay J. Reddi, Youfeng Wu, Jin Lee, Dan Connors, David Brooks, Margaret Martonosi, Douglas W. Clark. "A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance," *38th International Symposium on Microarchitecture*, November, 2005. **Best Paper Award. Selected as one of the Top Picks in Computer Architecture in 2005.**
- Xiaoyao Liang and David Brooks. "Highly Accurate Power Modeling Method for SRAM Structures with Simple Circuit Simulation," *IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers ($P = AC^2$)*, September, 2005.
- Yingmin Li, Mark Hempstead, Patrick Mauro, David Brooks, Zhigang Hu, and Kevin Skadron. "Power and Thermal Effects of SRAM vs. Latch-Mux Design Styles and Clock Gating Choices," *International Symposium on Low-Power Electronics and Design*, August, 2005.
- Mark Hempstead, Nikhil Tripathi, Patrick Mauro, Gu-Yeon Wei, David Brooks. "An Ultra Low Power System Architecture for Wireless Sensor Network Applications," *32nd International Symposium on Computer Architecture*, June, 2005.
- Yingmin Li, David Brooks, Zhigang Hu, Kevin Skadron. "Performance, Energy, and Thermal Considerations for SMT and CMP Architectures," *11th International Symposium on High-Performance Computer Architecture*, February, 2005.
- Yau Chin, John Sheu, and David Brooks. "Evaluating Techniques for Exploiting Instruction Slack," *22nd International Conference on Computer Design*, October, 2004.
- Yingmin Li, David Brooks, Zhigang Hu, and Kevin Skadron. "Evaluating the Thermal Efficiency of SMT and CMP Architectures," *IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers ($P = AC^2$)*, October, 2004.
- Kim Hazelwood and David Brooks. "Eliminating Voltage Emergencies via Microarchitectural Voltage Control Feedback and Dynamic Optimization," *International Symposium on Low-Power Electronics and Design*, August, 2004.

Yingmin Li, David Brooks, Zhigang Hu, Kevin Skadron, and Pradip Bose. "Understanding the Energy Efficiency of Simultaneous Multithreading," *International Symposium on Low-Power Electronics and Design*, August, 2004.

Russ Joseph, David Brooks, and Margaret Martonosi. "Control Techniques to Eliminate Voltage Emergencies in High-Performance Processors," *9th International Symposium on High-Performance Computer Architecture*, February, 2003.

Viji Srinivasan, David Brooks, Michael Gschwind, Pradip Bose, Victor Zyuban, Philip N. Strenski, and Philip G. Emma. "Optimizing Pipelines for Power and Performance," *35th International Symposium on Microarchitecture*, November, 2002. **Selected as one of the four Best IBM Research Papers in Computer Science, Electrical Engineering and Math published in 2002.**

Alper Buyuktosunoglu, Stanley Schuster, David Brooks, Pradip Bose, Peter Cook, David H. Albonese. "A Circuit Level Implementation of an Adaptive Issue Queue for Power-Aware Microprocessors," *11th Great Lakes Symposium on VLSI*, March, 2001.

David Brooks and Margaret Martonosi. "Dynamic Thermal Management for High-Performance Microprocessors," *Seventh International Symposium on High-Performance Computer Architecture*, January, 2001.

David Brooks, Vivek Tiwari, and Margaret Martonosi. "Wattch: A Framework for Architectural-Level Power Analysis and Optimizations," *27th International Symposium on Computer Architecture*, June, 2000.

David Brooks and Margaret Martonosi. "Dynamically Exploiting Narrow Width Operands to Improve Processor Power and Performance," *Fifth International Symposium on High-Performance Computer Architecture*, January, 1999.

BOOK, JOURNAL, MAGAZINE, AND NEWSLETTER PUBLICATIONS

Xiaoyao Liang, Ali Durlov Khan, David Brooks, and Gu-Yeon Wei. "Process-variation-tolerant systems via voltage interpolation and variable latency," *IEEE Journal of Solid-State Circuits*, **Under Preparation**.

Kevin Brownell, Ali Durlov Khan, Gu-Yeon Wei and David Brooks. "Assessment of Voltage Interpolation to Address Process Variations," *IEEE Transactions on VLSI*, **Accepted for Publication**.

Lukasz Stozek and David Brooks. "Efficient Architectures Through Application Clustering and Heterogeneity," *ACM Transactions on Architecture and Code Optimization*, Volume 6, No. 1, March, 2009.

Xiaoyao Liang, Gu-Yeon Wei, and David Brooks. "ReVIVaL: Variation Tolerant Microarchitecture," *IEEE Micro's Top Picks in Computer Architecture Conferences*, January/February, 2009.

Mark Hempstead, Michael J. Lyons, David Brooks and Gu-Yeon Wei. "Survey of Hardware Systems for Wireless Sensor Networks," *ASP Journal of Low Power Electronics*, Volume 4., No. 1, April, 2008.

Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, and David Brooks. "Replacing 6T SRAMs with 3T1D DRAMs in the L1 Data Cache to Combat Process Variability," *IEEE Micro's Top Picks in Computer Architecture Conferences*, January/February, 2008.

David Brooks, Robert Dick, Russ Joseph, and Li Shang. "Power, Thermal, and Reliability Modeling in Nanometer-Scale Microprocessors," *IEEE Micro's Special Issue: Hot Tutorials*, May/June, 2007.

Benjamin Lee and David Brooks. "A Tutorial in Spatial Sampling and Regression Strategies for Microarchitectural Analysis," *IEEE Micro's Special Issue: Hot Tutorials*, May/June, 2007.

Qiang Wu, Vijay J. Reddi, Youfeng Wu, Jin Lee, Dan Connors, David Brooks, Margaret Martonosi, Douglas W. Clark. "Dynamic Compiler Driven Control for Microprocessor Energy and Performance," *IEEE Micro's Top Picks in Computer Architecture Conferences*, January/February, 2006.

Victor Zyuban, David Brooks, Viji Srinivasan, Michael Gschwind, Pradip Bose, Philip N. Strenski, and Philip G. Emma. "Integrated Analysis of Power and Performance of Pipelined Microprocessors," *IEEE Transactions on Computers*, Volume 53, No. 8, August, 2004.

David Brooks, Pradip Bose, and Margaret Martonosi. "Power-Performance Simulation: Design and Validation Strategies," *ACM SIGMETRICS Performance Evaluation Review*, Volume 31, No. 4, March, 2004.

David Brooks, Pradip Bose, Viji Srinivasan, Michael Gschwind, Philip G. Emma, and Michael G. Rosenfield. "New Methodology for Early-Stage, Microarchitecture-Level Power-Performance Analysis of Microprocessors," *IBM Journal of Research and Development*, Volume 47, No. 5/6, Oct/Nov, 2003.

A. Buyuktosunoglu, D.H. Albonese, S. Schuster, D. Brooks, P. Bose, P. Cook. "Power-Efficient Issue Queue Design," In *Power Aware Computing*, R. Graybill and R. Melhem (Eds), Kluwer Academic Publishers, Chapter 3, pp. 37-60, 2002.

David Brooks, Pradip Bose, Stanley Schuster, Hans Jacobson, Prabhakar Kudva, Alper Buyuktosunoglu, John-David Wellman, Victor Zyuban, Manish Gupta, and Peter Cook. "Power-Aware Microarchitecture: Design and Modeling Challenges for Next Generation Microprocessors," *IEEE Micro*, November/December, 2000.

David Brooks, J.D. Wellman, Margaret Martonosi, and Pradip Bose. "Power-Performance Modeling and Tradeoff Analysis for a High End Microprocessor," *Workshop on Power Aware Computing Systems. (Associated with Symposium on Architectural Support for Programming Languages and Operating Systems.)* November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008.)

David Brooks and Margaret Martonosi. "Value-based Clock Gating and Operation Packing: Dynamic Strategies for Improving Processor Power and Performance," *ACM Transactions on Computer Systems*, Volume 18, No. 2, May, 2000.

REFEREED WORKSHOP PUBLICATIONS

Mark Hempstead, Gu-Yeon Wei and David Brooks. "Navigo: An early-stage model to study power-constrained architectures and specialization," *ISCA Workshop on Modeling, Benchmarking, and Simulations (MoBS)*, June, 2009.

Mark Hempstead, Gu-Yeon Wei and David Brooks. "An accelerator-based wireless sensor network processor in 130nm CMOS," *ISCA Workshop on Architectural Research Prototyping (WARP)*, June, 2009.

Vijay Janapa Reddi, Meeta S. Gupta, Krishna Rangan, Glenn Holloway, Gu-Yeon Wei, Michael D. Smith, and David Brooks. "Voltage Noise: Why It's Bad, and What To Do About It," *5th IEEE Workshop on Silicon Errors in Logic - System Effects (SELSE-5)*, March, 2009.

Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, and David Brooks. "Process Variation Tolerant Register Files Based on Dynamic Memories," *Workshop on Architectural Support for Gigascale Integration (ASGI-07) held with ISCA-34*, June, 2007.

Wonyoung Kim, Meeta S. Gupta, Gu-Yeon Wei and David Brooks. "Enabling On-Chip Switching Regulators for Multi-Core Processors Using Current Staggering," *Workshop on Architectural Support for Gigascale Integration (ASGI-07) held with ISCA-34*, June, 2007.

Benjamin C. Lee and David Brooks. "Statistically Rigorous Regression Modeling for the Microprocessor Design Space," *Workshop on Modeling, Benchmarking, and Simulation (MOBS'06) held with ISCA-33*, June, 2006.

Xiaoyao Liang and David Brooks. "Latency Adaptation for Multiported Register Files to Mitigate the Impact of Process Variations," *Workshop on Architectural Support for Gigascale Integration (ASGI-06) held with ISCA-33*, June, 2006.

Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, David Brooks. “Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications,” SRC Techcon, SoC Design Contest 2nd place, Portland, OR, October, 2005.

Benjamin Lee and David Brooks. “Effects of Pipeline Complexity on SMT/CMP Power-Performance Efficiency,” *Proceedings of the 6th Workshop on Complexity-Effective Design (WCED’05)*, June, 2005.

Mark Hempstead, David Brooks, Matt Welsh. “TinyBench: The Case For A Standardized Benchmark Suite for TinyOS Based Wireless Sensor Network Devices,” *Proceedings of the IEEE Workshop on Embedded Networked Sensors(EmNets’04)*, November, 2004.

Pradip Bose, David Brooks, Alper Buyuktosunoglu, Peter Cook, Kaushik Das, Philip Emma, Michael Gschwind, Hans Jacobson, Tejas Karkhanis, Stanley Schuster, Jim E. Smith, Viji Srinivasan, Victor Zyuban, David H. Albonesi, Sandhya Dwarkadas. “Early-Stage Definition of LPX: A Low Power Issue-Execute Processor Prototype,” *Workshop on Power Aware Computing Systems, Held at HPCA-8*, February, 2002.

David Brooks, J.D. Wellman, Margaret Martonosi, and Pradip Bose. “Power-Performance Modeling and Tradeoff Analysis for a High End Microprocessor,” *Workshop on Power Aware Computing Systems, at ASPLOS 2000*, November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008.)

Alper Buyuktosunoglu, Stanley Schuster, David Brooks, Pradip Bose, Peter Cook, David H. Albonesi. “An Adaptive Issue Queue for Reduced Power at High Performance,” *Workshop on Power Aware Computing Systems, at ASPLOS 2000*, November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008.)

David Brooks and Margaret Martonosi. “Adaptive Thermal Management for High-Performance Microprocessors,” *Proceedings of the 1st Workshop on Complexity-Effective Design (WCED’00)*, June, 2000.

David Brooks and Margaret Martonosi. “Implementing Application-Specific Cache Coherence Protocols in Configurable Hardware,” *Workshop on Communications, Architecture, and Applications for Network-based Parallel Computing, at HPCA-5*, January, 1999. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 1602.)

TUTORIALS AND SPECIAL CLASSES

David Brooks, with Keith Bowman, Gu-Yeon Wei, and Chris Wilkerson. “Design Variability: Trends, Models, and Design Solutions,” *41st Annual International Symposium on Microarchitecture (Micro-41)*, Lake Como, Italy, November, 2008.

David Brooks, with Bronis de Supinski, Benjamin C. Lee, Sally A. McKee, Martin Schulz, and Karan Singh. “Learning and Inference Tutorial (LIT) for Large Design and Parameter Spaces,” *13th International Conference on Architectural Support for Programming Languages and Operating Systems*, Seattle, WA, March, 2008.

David Brooks, with Bronis de Supinski, Benjamin Lee, Sally A. McKee, Martin Schulz, and Karan Singh. “Inference and Learning for Large Scale Microarchitectural Analysis,” *34th International Symposium on Computer Architecture*, San Diego, CA, June, 2007.

David Brooks. “Microarchitecture-Level Power Simulation: Modeling, Validation, and Design Impact,” *Cool Chips VIII*, Yokohama, Japan, April, 2005.

David Brooks, with Kevin Skadron, Antonio Gonzalez, Lev Finkelstein, and Mircea Stan. “Thermal Issues for Temperature-Aware Computer Systems,” *31st International Symposium on Computer Architecture*, Munich, Germany, June, 2004.

David Brooks, with Zhigang Hu and Victor Zyuban. “Microarchitecture-Level Power-Performance Simulators: Modeling, Validation, and Impact on Design,” *36th IEEE Symposium on Microarchitecture (MICRO-36)*, San Diego, CA, December, 2003.

David Brooks, with Kevin Skadron and Mircea Stan. “Thermal Management Issues for Microprocessors,” *35th IEEE Symposium on Microarchitecture (MICRO-35)*, Istanbul, Turkey, November, 2002.

David Brooks, with Pradip Bose, Mary Jane Irwin, Mahmut Kandemir, Margaret Martonosi, and Vijaykrishnan Narayanan. “Power-Efficient Design: Modeling and Optimizations,” *28th International Symposium on Computer Architecture*, Gotenburg, Sweden, June, 2001.

David Brooks, with Pradip Bose and Margaret Martonosi. “Power-Performance Modeling, Analysis and Validation,” *Seventh IEEE Symposium on High-Performance Computer Architecture (HPCA-7)*, Monterrey, Mexico, January, 2001.

David Brooks, with Pradip Bose and Margaret Martonosi. “Modeling and Analyzing CPU Power and Performance: Metrics, Methods, and Abstractions,” *ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems*, Cambridge, MA, June, 2001.

INVITED TALKS

“Architectural Energy Efficiency,” Invited Talk: 2009 Symposium on VLSI Circuits, Short Course on Energy Management for Green SoC’s and SiP’s, June, 2009.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at University of Massachusetts – Amherst, February, 2009.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Massachusetts Institute of Technology, December, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Brown University, December, 2008.

“Architectures for wireless sensor node design,” Presented at Politecnico di Milano, November, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Stanford University, October, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Intel, Portland, Oregon. September, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at University of Texas, Austin, September, 2008.

“Synergistic Supply Voltage Control and Management in the Multicore Era,” Presented at HP Labs, Palo Alto, California, September, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Universitat Politecnica de Catalunya, and Intel Barcelona Research Center, July, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at IBM T.J. Watson Research Center, July, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Tsinghua University, Beijing, China, June, 2008

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at University of California, Berkeley, May, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at University of Illinois, Urbana-Champaign, April, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at University of Michigan, April, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at North Carolina State University, April, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Duke University, April, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at University of Wisconsin, Madison, March, 2008.

“Computer Design in the Nanometer Scale Era: Challenges and Solutions,” Presented at Intel, Hudson, Massachusetts, March, 2008.

“Reducing the Energy Footprint of Data Centers Panel,” Presented at VMworld, September, 2007.

“Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications,” Presented at Chalmers University of Technology, June, 2007.

“Architectural Approaches to Technology-Driven Computer Design,” Presented at Carnegie Mellon University, October, 2006.

“Architectural Approaches to Technology-Driven Computer Design,” Presented at Lawrence Livermore National Laboratory, August, 2006.

“Architectural Approaches to Technology-Driven Computer Design,” Presented at IBM T.J. Watson Research Center, May, 2006.

“Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications,” Presented at Princeton University, November, 2005.

“Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications,” Presented at Penn State University, September, 2005.

“Performance, Energy, and Thermal Considerations for SMT and CMP Architectures,” Presented at Intel, Hudson, Massachusetts, March, 2005.

“Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications,” Presented at Boston University, March, 2005.

“Pushing the Bounds of Low-Power Computing: An Event-Driven Architecture for Sensor Network Applications,” Presented at University of Connecticut, March, 2005.

“Pushing the Bounds of Low-Power Computing,” Presented at IBM Research, Yorktown Heights, NY, January, 2005.

“Adaptive Alarm-Based Approaches to High-Performance/Low-Cost Computing,” Presented at Harvard Industrial Partnership Meeting, October, 2004.

“Computer Architecture for Thermal Management,” Presented at Harvard Applied Mechanics and Mathematics Study Group.

“Power-Aware Computing: Background, Modeling, and Design,” Presented to Intel VSSAD, Hudson, MA, April, 2004.

“Power-aware Computing: Applications and Architectures,” Presented at Harvard Industrial Partnership Meeting, November, 2003.

“Architectural and System Level Power Analysis and Optimization,” Presented at the Low-Power Circuit and System Design Workshop, International Conference on Computer Design, September, 2003.

“Optimizing Pipelines for Power and Performance,” Presented to Intel VSSAD, Hudson, MA, February, 2003.

SOFTWARE AND TOOLS

David Brooks and Margaret Martonosi. *wattch*. An Architectural-Level Power-Performance Analysis Toolkit. 2000

PATENTS

Process Variation Tolerant Circuit With Voltage Interpolation And Variable Latency, Patent Application #: 12,261,771, Filed Oct. 2008.

Ultra Low Power System for Sensor Network Applications, Patent Application #: 11,685,721, Filed Mar. 2007.

Processor with Low Overhead Predictive Supply Voltage Gating for Leakage Power Reduction, US Patent #: 7,134,028, Granted 2006.

System and Method of Operand Value Based Processor Optimization by Detecting a Condition of Pre-Determined Number of Bits and Selectively Disabling Pre-Determined Bit-Fields by Clock Gating, US Patent #: 6,745,336, Granted 2004.

Memory Structures Having Selectively Disabled Portions for Power Conservation, US Patent #: 6,298,002, Granted 2001, US Patent #: 6,473,326, Granted 2002, US Patent #: 6,577,524, Granted 2003.

Adaptive Issue Queue for Reduced Power at High Performance, Filed 2001.

RESEARCH FUNDING

Research Grants

National Science Foundation and Semiconductor Research Corporation, co-PI (PI is Gu-Yeon Wei), “Flexible voltage stacking for chip multiprocessors,” 2009–2012.

Semiconductor Research Corporation, Principal Investigator (co-PI is Gu-Yeon Wei), “Scalable Pre-RTL Power Modeling Infrastructure for MP-SOC Architectures,” 2008–2011.

National Science Foundation, Principal Investigator (co-PIs are Robert Dick, Russ Joseph, and Gu-Yeon Wei), CCF-0720566, “Integrated Power Delivery - Hardware-Software Techniques to Eliminate Off-Chip Regulation from Embedded Systems,” 2007–2011.

National Science Foundation, Principal Investigator (co-PI is Gu-Yeon Wei), CCF-0702344, “Reliability in the Face of Variability under Nanoscale Technology Scaling,” 2007–2010.

Defense Advanced Research Projects Agency, Principal Investigator (Young Faculty Award), “Microwatt Computing – Application-Driven Architectures for Wireless Sensor Devices,” 2007.

National Science Foundation, Principal Investigator, CCF-0448313, “CAREER: A Framework for Early-Stage Computer Architecture Design Space Exploration and Optimization,” 2005–2010.

National Science Foundation, Principal Investigator (co-PIs are Gu-Yeon Wei and Michael Smith), CCF-0429782, “An Adaptive Alarm-Based Approach to High-Performance/Low-Cost Computing”, 2004–2007.

National Science Foundation, co-PI (PI is Margo Seltzer, other co-PIs are Wei, Kung, Tarokh), SCI-0330244, “SENSORS: Hourglass: An Infrastructure for Sensor Network”, 2003–2007.

Research Gifts

Microsoft Corporation Research Gift, Principal Investigator (co-PIs are Gu-Yeon Wei and Michael Smith), “A Synergistic Approach To Adaptive Power Management,” 2008.

Intel Research Gift, Principal Investigator (co-PI is Michael Smith), “Integrated, Software-Managed Power and Reliability for Next-Generation CMP machines,” 2007–2009.

Intel Research Gift, Principal Investigator (co-PI is Gu-Yeon Wei), “Reliability in the face of variability under nanoscale technology scaling,” 2007–2009.

Sun Microsystems Research Gift, Co-Principal Investigator (PI is Gu-Yeon Wei), “Advanced memory design in deep submicron technologies,” 2007–2009.

Semiconductor Research Association SoC Design Challenge, 1st Prize Award in Phase 2 includes cash prize and design fabrication on IBM .18um process (submission co-lead with Gu-Yeon Wei), 2006.

Harvard Cooke/Clark Fund, “Software-Managed Power Management for Next-Generation Chip Multiprocessors,” 2005–2007.

Catalyst Foundation, “ μ Watt Computing - Application-Driven Circuits and Architectures for Wireless Sensor Devices,” 2005–2006.

Intel Research Gift, Principal Investigator, “Thermal-Aware Microprocessor Design: Studying the Impact of Advanced Cooling Technologies on Chip Floorplans and Microarchitecture,” 2004–2007.

IBM Faculty Partnership Award, 2003–2005.

Equipment/Software Donations

Analog Devices Equipment Donation, ADI Test Boards, 2008.

SRC Design Contest, Chip Fabrication Expenses, 2005.

UNIVERSITY TEACHING

Harvard University. Computer Science 141: Computing Hardware. Digital Logic Design and Basic Computer Architecture. Fall 2005, Fall 2006, Fall 2007, Fall 2008.

Harvard University. Computer Science 146: Computer Architecture. Introduction to Quantitative Approach to Computer Architecture. Fall 2002, Spring 2004, Spring 2005.

Harvard University. Computer Science 246: Advanced Computer Architecture. Power-Aware Computer Systems Graduate Course and Design Projects. Spring 2003, Fall 2003, Fall 2004, Spring 2006, Spring 2007, Spring 2008, Spring 2009.

RESEARCH ADVISING

Doctoral Students

Yingmin Li, Computer Science, PhD 2006, University of Virginia (co-advised with Kevin Skadron)
Thesis Title: “Physical Constraints Aware Chip Multiprocessor Architecture”

Benjamin Lee, Computer Science, PhD 2008, Harvard University
Thesis Title: “Statistical Inference for Efficient Microarchitectural Analysis”

Xiaoyao Liang, Electrical Engineering, PhD 2008, Harvard University
Thesis title: “Joint Architecture and Circuit Resilience to Mitigate the Impact of Process Variations”

Mark Hempstead, Electrical Engineering, PhD 2009, Harvard University
Thesis title: “Accelerator-Based Architectures for Wireless Sensor Network Applications”

Meeta Gupta, Electrical Engineering, PhD Expected Fall 2009, Harvard University

Mike Lyons, Computer Science, Post-Quals, Harvard University

Krishna Rangan, Electrical Engineering, Post-Quals, Harvard University

Vijay Janapa (VJ) Reddi, Computer Science, Post-Quals, Harvard University

Wonyoung Kim, Electrical Engineering, Post-Quals, Harvard University (secondary advisor)

Kevin Brownell, Electrical Engineering, Pre-Quals, Harvard University

Jian Li, Electrical Engineering, Pre-Quals, Harvard University (secondary advisor)

Nikhil Tripathi, Computer Science, Harvard University (2003–2005)

Undergraduate and Masters Students

Kristen Lovin, AB/SM 2008, Harvard University, Advised from 2005–2008.

Durlov Khan, SM 2008, Harvard University, Advised from 2007–2008.

Patrick Mauro, AB 2007, Harvard University, Advised in 2004.

Lukasz Stozek, AB/SM 2006, Harvard University, Advised from 2005–2006.

Jarod Oatley, SM 2006, Harvard University, Advised from 2005–2006.

John Sheu, AB 2004, Harvard University, Advised from 2003–2004.

Yau Chin, AB 2004, Harvard University, Advised from 2003–2004.

VISITORS AND RESEARCH STAFF

Glenn Holloway, 2006–Present (Research Staff)

Simone Campanoni, 2008 (PhD student visiting from Politecnico di Milano, advisor Professor Stefano Crespi Reghizzi)

Ramon Canal, 2006–2007 (Visiting Faculty Member from UPC-Barcelona)

Jiyang Kang, 2006–2007 (Visiting Researcher from Samsung Corporation)

UNIVERSITY SERVICE

Director of Undergraduate Studies, Computer Science, 2004–2007.

Committee Member, Committee on Graduate Admissions and Scholarship, 2002–2007.

Committee Member, Computer Science Committee on Undergraduate Studies, 2002–Present.

Committee Member, Engineering Sciences Committee on Undergraduate Studies, 2002–2005.

Committee Member, Computer Science Junior Faculty Search Committee, Spring 2003.

Committee Member, Committee on Higher Degrees, 2002–2003.

Thesis Committee Member for several Ph.D. Students.

Qualifying Exam Committee Member for several Ph.D. Students.

PROFESSIONAL SERVICE

Conference Organization Activities

Program Chair, International Symposium on Performance Analysis of Systems and Software, 2010.

Program Committee, International Symposium on High-Performance Computer Architecture, 2010.

Program Committee, International Symposium on Computer Architecture, 2009.

Workshops/Tutorials Co-Chair, International Symposium on Microarchitecture, 2009.

External Program Committee, International Symposium on Programming Language Design and Implementation, 2009.

Steering Committee, NSF Workshop on Science of Power Management, 2009.

Program Committee, Special Issue of IEEE Micro's Top Picks from Computer Architecture Conferences, 2009.

Program Committee, International Symposium on High-Performance Computer Architecture, 2009.

Program Committee, International Conference on Parallel Architectures and Compilation Techniques, 2009.

Program Committee, International Symposium on Low Power Electronics and Design, 2009.

Program Committee, International Conference on Computer Design, 2009.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2009.

Vice Program Chair, Computer Architecture Track, International Symposium on Computer Architecture and High-Performance Computing, 2009

Program Committee, International Parallel and Distributed Processing Symposium, 2009.

Program Committee, International Symposium on High-Performance Computer Architecture, 2008.

Program Committee, International Symposium on Low Power Electronics and Design, 2008.

Program Committee, ACM International Conference on Computing Frontiers, 2008.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2008

Technical Program Committee Co-Chair, Special Issue of IEEE Micro Micro's Top Picks from Computer Architecture Conferences, 2008.

Program Committee, International Symposium on Microarchitecture, 2007.

Program Committee, International Symposium on Low Power Electronics and Design, 2007.

Publication Chair and Program Committee, International Symposium on Performance Analysis of Systems and Software, 2007.

Program Vice-Chair, and Program Committee, Technology-Driven Architectures, ACM International Conference on Computing Frontiers, 2007.

Program Committee, Special Issue of IEEE Micro Micro's Top Picks from Computer Architecture Conferences, 2007.

Program Committee, International Symposium on High-Performance Computer Architecture, 2007.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2007.

Program Committee, International Conference on Architectural Support for Programming Languages and Operating Systems, 2006.

Track Co-chair (with Michael Gschwind), Processor Architecture Track, International Conference on Computer Design, 2006.

Program Committee, International Symposium on High-Performance Computer Architecture, 2006.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2006.

Program Committee, International Parallel and Distributed Processing Symposium, 2006.

Program Committee, International Conference on Parallel and Distributed Systems, 2006.

Track Co-chair (with Michael Gschwind), Processor Architecture Track, International Conference on Computer Design, 2005.

Program Committee, International Symposium on Low Power Electronics and Design, 2005.

Program Committee, International Conference on Computer Design, 2004.

Registration and Finance Chair, International Symposium on Microarchitecture, 2004.

Program Committee, International Symposium on Low Power Electronics and Design, 2004.

Program Committee, International Conference on Computer Design, 2003.

Program Committee, International Symposium on High-Performance Computer Architecture, 2003.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2002.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2001.

Web and Publicity Co-Chair, International Symposium on Performance Analysis of Systems and Software, 2001.

Journal Review Activities

IEEE Journal of Solid-State Circuits (JSSC)

IEEE Transactions on Very Large Scale Integration Systems (TVLSI)

IEEE Transactions on Computers

IEEE Transactions on Computer-Aided Design

IEEE Transactions on Parallel and Distributed Systems
IEEE Micro
IEEE Computer
IEEE Computer Architecture Letters
IEEE Pervasive Computing
ACM Transactions on Architecture and Code Optimization
ACM Transactions on Design Automation of Electronic Systems
ACM Transactions on Embedded Computer Systems
ACM Transactions on Sensor Networks
ACM Journal of Emerging Technologies in Computing
Journal of Parallel and Distributed Computing.
IET Computers and Digital Techniques

Grant Review Activities

Two NSF Panels in 2009
Two NSF Panels in 2008
One NSF Panel in 2006
One NSF Panel in 2005