

# David M. Brooks

School of Engineering and Applied Sciences  
Maxwell-Dworkin Laboratories, Room 141  
33 Oxford Street  
Cambridge, MA 02138

dbrooks@eecs.harvard.edu  
www.eecs.harvard.edu/~dbrooks/  
Phone: (617) 495-3989  
Fax: (617) 495-2489

## EDUCATION

- Princeton University.** Doctor of Philosophy in Electrical Engineering, 2001.
- Princeton University.** Master of Arts in Electrical Engineering, 1999.
- University of Southern California.** Bachelor of Science in Electrical Engineering, 1997.

## ACADEMIC AND PROFESSIONAL EXPERIENCE

**Associate Professor of Computer Science**, School of Engineering and Applied Sciences, Harvard University (07/06 - Present).

- Areas of Interest: Computer Architecture, Embedded and High-Performance Computer System Design.
- Pursuing research in computer architectures and the hardware/software interface, particularly power-efficient and temperature-aware computer systems and architectural-level power modeling.

**Assistant Professor of Computer Science**, Division of Engineering and Applied Sciences, Harvard University (9/02 - 07/06).

**Research Staff Member**, IBM T.J. Watson Research Center, (9/01 - 9/02).

- Conducted analysis for the optimal power-performance pipeline depth of microprocessors.
- Continued development of IBM PowerTimer toolkit for architectural power-performance modeling.
- Assisted in concept-phase and high-level design phase power-performance analysis for the Sony-Toshiba-IBM Cell Processor.

**Research Assistant**, Princeton University, (7/97 - 9/01).

- Investigated the potential for dynamic thermal management in microprocessor designs.
- Developed the Wattch architectural power-modeling toolkit.
- Investigated the potential for narrow-width bitwidth optimizations for power-performance optimizations in ALUs and functional units.

**Research Intern**, IBM T.J. Watson Research Center, (6/00 - 9/00).

**Research Intern**, Intel Corporation, (6/99 - 9/99).

## HONORS AND AWARDS

- DARPA/MTO Young Faculty Award, 2007.
- 1st Prize, Phase 2 of SRC SoC Design Challenge, October, 2006.
- 2nd Prize, Phase 1 of SRC SoC Design Challenge, October, 2005.
- National Science Foundation CAREER Award, February, 2005.
- IBM Faculty Partnership Award, 2004-05.
- National Science Foundation Graduate Research Fellow, 1998-2001.

Princeton University Gordon Wu Graduate Fellow, 1997-2001.

University of Southern California Trustee Scholar, 1993-1997.

#### REFEREED CONFERENCE PUBLICATIONS

Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, and David Brooks. "Process Variation Tolerant 3T1D-Based Cache Architectures," *40th International Symposium on Microarchitecture*, December, 2007.

Xiaoyao Liang, Kerem Turgay, and David Brooks. "Architectural Power Models for SRAM and CAM Structures Based on Hybrid Analytical/Empirical Techniques," *International Conference on Computer Aided Design*, November, 2007.

Meeta S. Gupta, Krishna K. Rangan, Mike D. Smith, Gu-Yeon Wei, and David M. Brooks. "Towards a Software Approach to Mitigate Voltage Emergencies," *International Symposium on Low Power Electronics and Design*, August, 2007.

Meeta S. Gupta, Jarod L. Oatley, Russ Joseph, Gu-Yeon Wei, and David Brooks. "Understanding Voltage Variations in Chip Multiprocessors using a Distributed Power-Delivery Network," *10th Design, Automation, and Test in Europe Conference*, April, 2007.

Benjamin Lee, David Brooks, Bronis de Supinski, Martin Schulz, Karan Singh, and Sally McKee. "Methods of Inference and Learning for Performance Modeling of Parallel Applications," *Symposium on Principles and Practice of Parallel Programming*, March, 2007.

Benjamin Lee and David Brooks. "Illustrative Design Space Studies with Microarchitectural Regression Models," *13th International Symposium on High-Performance Computer Architecture*, February, 2007.

Xiaoyao Liang and David Brooks. "Mitigating the Impact of Process Variations on CPU Register File and Execution Units," *39th International Symposium on Microarchitecture*, December, 2006.

Xiaoyao Liang and David Brooks. "Microarchitecture Parameter Selection to Optimize System Performance under Process Variation," *International Conference on Computer Aided Design*, November, 2006.

Benjamin Lee and David Brooks. "Accurate and Efficient Regression Modeling for Microarchitectural Performance and Power Prediction," *International Conference on Architectural Support for Programming Languages and Operating Systems*, October, 2006.

Lukasz Stozek and David Brooks. "Efficient Architectures through Application Clustering and Architectural Heterogeneity," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October, 2006.

Mark Hempstead, Gu-Yeon Wei, and David Brooks. "Architecture and Circuit Techniques for Low Throughput, Energy Constrained Systems Across Technology Generations," *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems*, October, 2006.

Yingmin Li, Benjamin Lee, David Brooks, Zhigang Hu, Kevin Skadron. "CMP Design Space Exploration Subject to Physical Constraints," *12th International Symposium on High-Performance Computer Architecture*, February, 2006.

Qiang Wu, Vijay J. Reddi, Youfeng Wu, Jin Lee, Dan Connors, David Brooks, Margaret Martonosi, Douglas W. Clark. "A Dynamic Compilation Framework for Controlling Microprocessor Energy and Performance," *38th International Symposium on Microarchitecture*, November, 2005. Received Best Paper Award.

Xiaoyao Liang and David Brooks. "Highly Accurate Power Modeling Method for SRAM Structures with Simple Circuit Simulation," *IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers ( $P = AC^2$ )*, September, 2005.

Yingmin Li, Mark Hempstead, Patrick Mauro, David Brooks, Zhigang Hu, and Kevin Skadron. "Power and Thermal Effects of SRAM vs. Latch-Mux Design Styles and Clock Gating Choices," *International Symposium on Low-Power Electronics and Design*, August, 2005.

Mark Hempstead, Nikhil Tripathi, Patrick Mauro, Gu-Yeon Wei, David Brooks. "An Ultra Low Power System Architecture for Wireless Sensor Network Applications," *32nd International Symposium on Computer Architecture*, June, 2005.

Yingmin Li, David Brooks, Zhigang Hu, Kevin Skadron. "Performance, Energy, and Thermal Considerations for SMT and CMP Architectures," *11th International Symposium on High-Performance Computer Architecture*, February, 2005.

Yau Chin, John Sheu, and David Brooks. "Evaluating Techniques for Exploiting Instruction Slack," *22nd International Conference on Computer Design*, October, 2004.

Yingmin Li, David Brooks, Zhigang Hu, and Kevin Skadron. "Evaluating the Thermal Efficiency of SMT and CMP Architectures," *IBM Watson Conference on Interaction between Architecture, Circuits, and Compilers ( $P = AC^2$ )*, October, 2004.

Kim Hazelwood-Cettei and David Brooks. "Eliminating Voltage Emergencies via Microarchitectural Voltage Control Feedback and Dynamic Optimization," *International Symposium on Low-Power Electronics and Design*, August, 2004.

Yingmin Li, David Brooks, Zhigang Hu, Kevin Skadron, and Pradip Bose. "Understanding the Energy Efficiency of Simultaneous Multithreading," *International Symposium on Low-Power Electronics and Design*, August, 2004.

Russ Joseph, David Brooks, and Margaret Martonosi. "Control Techniques to Eliminate Voltage Emergencies in High-Performance Processors," *International Symposium on High-Performance Computer Architecture*, January, 2003.

Viji Srinivasan, David Brooks, Michael Gschwind, Pradip Bose, Victor Zyuban, Philip N Strenski, and Philip G Emma. "Optimizing Pipelines for Power and Performance," *35th International Symposium on Microarchitecture*, November, 2002.

Alper Buyuktosunoglu, Stanley Schuster, David Brooks, Pradip Bose, Peter Cook, David H. Albonese. "A Circuit Level Implementation of an Adaptive Issue Queue for Power-Aware Microprocessors," *11th Great Lakes Symposium on VLSI*, March, 2001.

David Brooks and Margaret Martonosi. "Dynamic Thermal Management for High-Performance Microprocessors," *Seventh International Symposium on High-Performance Computer Architecture*, January, 2001.

David Brooks, Vivek Tiwari, and Margaret Martonosi. "Wattch: A Framework for Architectural-Level Power Analysis and Optimizations," *27th International Symposium on Computer Architecture*, June, 2000.

David Brooks and Margaret Martonosi. "Dynamically Exploiting Narrow Width Operands to Improve Processor Power and Performance," *Fifth International Symposium on High-Performance Computer Architecture*, January, 1999.

#### BOOK, JOURNAL, MAGAZINE, AND NEWSLETTER PUBLICATIONS

David Brooks, Robert Dick, Russ Joseph, and Li Shang. "Power, Thermal, and Reliability Modeling in Nanometer-Scale Microprocessors," *IEEE MICRO's Special Issue: Hot Tutorials*, May/June 2007.

Benjamin Lee and David Brooks. "A Tutorial in Spatial Sampling and Regression Strategies for Microarchitectural Analysis," *IEEE MICRO's Special Issue: Hot Tutorials*, May/June 2007.

Qiang Wu, Vijay J. Reddi, Youfeng Wu, Jin Lee, Dan Connors, David Brooks, Margaret Martonosi, Douglas W. Clark. "Dynamic Compiler Driven Control for Microprocessor Energy and Performance," *IEEE MICRO's Top Picks in Computer Architecture Conferences*, January/February, 2006.

Victor Zyuban, David Brooks, Viji Srinivasan, Michael Gschwind, Pradip Bose, Philip N Strenski, and Philip G Emma. "Integrated Analysis of Power and Performance of Pipelined Microprocessors," *IEEE Transactions on Computers*, Volume 53, No. 8, August, 2004.

David Brooks, Pradip Bose, and Margaret Martonosi. "Power-Performance Simulation: Design and Validation Strategies," *ACM SIGMETRICS Performance Evaluation Review*, Volume 31, No. 4, March, 2004.

David Brooks, Pradip Bose, Viji Srinivasan, Michael Gschwind, Philip G. Emma, and Michael G. Rosenfield. "New Methodology for Early-Stage, Microarchitecture-Level Power-Performance Analysis of Microprocessors," *IBM Journal of Research and Development*, Volume 47, No. 5/6, Oct/Nov, 2003.

A. Buyuktosunoglu, D.H. Albonesi, S. Schuster, D. Brooks, P. Bose, P. Cook. "Power-Efficient Issue Queue Design," In *Power Aware Computing*, R. Graybill and R. Melhem (Eds), Kluwer Academic Publishers, Chapter 3, pp. 37-60, 2002.

David Brooks, Pradip Bose, Stanley Schuster, Hans Jacobson, Prabhakar Kudva, Alper Buyuktosunoglu, John-David Wellman, Victor Zyuban, Manish Gupta, and Peter Cook. "Power-Aware Microarchitecture: Design and Modeling Challenges for Next Generation Microprocessors," *IEEE Micro*, November/December, 2000.

David Brooks, J.D. Wellman, Margaret Martonosi, and Pradip Bose. "Power-Performance Modeling and Tradeoff Analysis for a High End Microprocessor," *Workshop on Power Aware Computing Systems. (Associated with Symposium on Architectural Support for Programming Languages and Operating Systems.)* November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008)

David Brooks and Margaret Martonosi. "Value-based Clock Gating and Operation Packing: Dynamic Strategies for Improving Processor Power and Performance," *ACM Transactions on Computer Systems*, Volume 18, No. 2, May, 2000.

#### REFEREED WORKSHOP PUBLICATIONS

Xiaoyao Liang, Ramon Canal, Gu-Yeon Wei, and David Brooks. "Process Variation Tolerant Register Files Based on Dynamic Memories," *Workshop on Architectural Support for Gigascale Integration (ASGI-07) held with ISCA-34*, June, 2007.

Benjamin C. Lee and David Brooks. "Statistically Rigorous Regression Modeling for the Microprocessor design space," *Workshop on Modeling, Benchmarking, and Simulation (MOBS'06) held with ISCA-33*, June, 2006.

Xiaoyao Liang and David Brooks. "Latency Adaptation for Multiported Register Files to Mitigate the Impact of Process Variations," *Workshop on Architectural Support for Gigascale Integration (ASGI-06) held with ISCA-33*, June, 2006.

Mark Hempstead, Xiaoyao Liang, Patrick Mauro, Gu-Yeon Wei, David Brooks. "Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications," SRC Techcon, SoC Design Contest 2nd place, Portland, OR, October 2005.

Benjamin Lee and David Brooks. "Effects of Pipeline Complexity on SMT/CMP Power-Performance Efficiency," *Proceedings of the 6th Workshop on Complexity Effective Design (WCED'05)*, June, 2005.

Mark Hempstead, David Brooks, Matt Welsh. "TinyBench: The Case For A Standardized Benchmark Suite for TinyOS Based Wireless Sensor Network Devices," *Proceedings of the IEEE Workshop on Embedded Networked Sensors(EmNets'04)*, November, 2004.

Pradip Bose, David Brooks, Alper Buyuktosunoglu, Peter Cook, Kaushik Das, Philip Emma, Michael Gschwind, Hans Jacobson, Tejas Karkhanis, Stanley Schuster, Jim E. Smith, Viji Srinivasan, Victor Zyuban, David H. Albonesi, Sandhya Dwarkadas. "Early-Stage Definition of LPX: A Low Power Issue-Execute Processor Prototype," *Workshop on Power Aware Computing Systems, Held at HPCA-8*, February, 2002.

David Brooks, J.D. Wellman, Margaret Martonosi, and Pradip Bose. "Power-Performance Modeling and Tradeoff Analysis for a High End Microprocessor," *Workshop on Power Aware Computing*

*Systems*, at *ASPLOS 2000*, November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008)

Alper Buyuktosunoglu, Stanley Schuster, David Brooks, Pradip Bose, Peter Cook, David H. Albonese. "An Adaptive Issue Queue for Reduced Power at High Performance," *Workshop on Power Aware Computing Systems*, at *ASPLOS 2000*, November, 2000. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 2008)

David Brooks and Margaret Martonosi. "Adaptive Thermal Management for High-Performance Microprocessors," *Proceedings of the 1st Workshop on Complexity Effective Design (WCED'00)*, June, 2000.

David Brooks and Margaret Martonosi. "Implementing Application-Specific Cache Coherence Protocols in Configurable Hardware," *Workshop on Communications, Architecture, and Applications for Network-based Parallel Computing*, at *HPCA-5*, January, 1999. (Also in Springer-Verlag Lecture Notes in Computer Science Volume 1602)

#### TUTORIALS AND SPECIAL CLASSES

David Brooks, with Bronis de Supinski, Benjamin Lee, Sally A. McKee, Martin Schulz, and Karan Singh. "Inference and learning for large scale microarchitectural analysis," *34th International Symposium on Computer Architecture*, San Diego, CA, June, 2007.

David Brooks, with Kevin Skadron, Antonio Gonzalez, Lev Finkelstein, and Mircea Stan. "Thermal Issues for Temperature-Aware Computer Systems," *31st International Symposium on Computer Architecture*, Munich, Germany, June, 2004.

David Brooks. "Microarchitecture-level Power Simulation: Modeling, Validation, and Design Impact," *Cool Chips VIII*, Yokohama, Japan, April, 2005.

David Brooks, with Kevin Skadron, Antonio Gonzalez, Lev Finkelstein, and Mircea Stan. "Thermal Issues for Temperature-Aware Computer Systems," *31st International Symposium on Computer Architecture*, Munich, Germany, June, 2004.

David Brooks, with Zhigang Hu and Victor Zyuban. "Microarchitecture-Level Power-Performance Simulators: Modeling, Validation, and Impact on Design," *36th IEEE Symposium on Microarchitecture (MICRO-36)*, San Diego, CA, December, 2003.

David Brooks, with Kevin Skadron and Mircea Stan. "Thermal Management Issues for Microprocessors," *35th IEEE Symposium on Microarchitecture (MICRO-35)*, Istanbul, Turkey, November, 2002.

David Brooks, with Pradip Bose, Mary Jane Irwin, Mahmut Kandemir, Margaret Martonosi, and Narayanan Vijaykrishnan. "Power-Efficient Design: Modeling and Optimizations," *28th International Symposium on Computer Architecture*, Gotenburg, Sweden, June, 2001.

David Brooks, with Pradip Bose and Margaret Martonosi. "Power-Performance Modeling, Analysis and Validation," *Seventh IEEE Symposium on High-Performance Computer Architecture (HPCA-7)*, Monterrey, Mexico, January, 2001.

David Brooks, with Pradip Bose and Margaret Martonosi. "Modeling and Analyzing CPU Power and Performance: Metrics, Methods, and Abstractions," *ACM SIGMETRICS Conference on Measurement and Modeling of Computer Systems*, Cambridge, MA, June, 2001.

#### INVITED TALKS

"Reducing the Energy Footprint of Data Centers Panel," Presented at VMworld, September, 2007.

"Pushing the bounds of low-power computing: An Event-driven Architecture for Sensor Network Applications," Presented at Chalmers University of Technology, June, 2007.

"Architectural Approaches to Technology-Driven Computer Design," Presented at Carnegie Mellon University, October, 2006.

“Architectural Approaches to Technology-Driven Computer Design,” Presented at Lawrence Livermore National Laboratory, August, 2006.

“Architectural Approaches to Technology-Driven Computer Design,” Presented at IBM T.J. Watson Research Center, May, 2006.

“Pushing the bounds of low-power computing: An event-driven architecture for sensor network applications,” Presented at Princeton University, November, 2005.

“Pushing the bounds of low-power computing: An event-driven architecture for sensor network applications,” Presented at Penn State University, September, 2005.

“Performance, Energy, and Thermal Considerations for SMT and CMP Architectures,” Presented at Intel, Hudson, MA, March, 2005.

“Pushing the bounds of low-power computing: An event-driven architecture for sensor network applications,” Presented at Boston University, March, 2005.

“Pushing the bounds of low-power computing: An event-driven architecture for sensor network applications,” Presented at University of Connecticut, March, 2005.

“Pushing the bound of low-power computing,” Presented at IBM Research, Yorktown Heights, NY, January, 2005.

“Adaptive Alarm-Based Approaches to High-Performance/Low-Cost Computing,” Presented at Harvard Industrial Partnership Meeting, October, 2004.

“Computer architecture for thermal management,” Presented at Harvard Applied Mechanics and Mathematics Study Group.

“Power-Aware Computing: Background, Modeling, and Design,” Presented to Intel VSSAD, Hudson, MA, April, 2004.

“Power-aware Computing: Applications and Architectures,” Presented at Harvard Industrial Partnership Meeting, November, 2003.

“Architectural and System Level Power Analysis and Optimization,” Presented at the Low-Power Circuit and System Design Workshop, International Conference on Computer Design, September, 2003.

“Optimizing Pipelines for Power and Performance,” Presented to Intel VSSAD, Hudson, MA, February, 2003.

#### SOFTWARE AND TOOLS

David Brooks and Margaret Martonosi. *wattch*. An Architectural-Level Power-Performance Analysis Toolkit. 2000

#### PATENTS

P. Bose, D. Brooks, P. Cook, P. Emma, M. Gschwind, S. Schuster, V. Srinivasan, *Processor with low overhead predictive supply voltage gating for leakage power reduction*, US Patent #7,134,028, Granted 2006.

M. Martonosi and D. Brooks, *System and method of operand value based processor optimization by detecting a condition of pre-determined number of bits and selectively disabling pre-determined bit-fields by clock gating*, US Patent #6,745,336, Granted 2004.

D. Brooks and V. Tiwari, *Memory Structures Having Selectively Disabled Portions for Power Conservation*, US Patent #6,298,002, Granted 2001, US Patent #6,473,326, Granted 2002, US Patent #6,577,524, Granted 2003.

A. Buyuktosunoglu, S. Schuster, D. Brooks, P. Bose, P. Cook, D. Albonesi, *Adaptive issue queue for reduced power at high performance*, Filed 2002.

## RESEARCH FUNDING

Intel Research Gift, Principal Investigator (co-PI is Mike Smith), “Integrated, Software-Managed Power and Reliability for Next-Generation CMP machines,” 2007-2009.

National Science Foundation, Principal Investigator (co-PI are Robert Dick, Russ Joseph, and Gu-Yeon Wei), CCF-0720566, “Integrated Power Delivery - Hardware-Software Techniques to Eliminate Off-Chip Regulation from Embedded Systems,” 2007-2011.

National Science Foundation, Principal Investigator (co-PI is Gu-Yeon Wei), CCF-0702344, “Reliability in the Face of Variability under Nanoscale Technology Scaling,” 2007-2010.

Defense Advanced Research Projects Agency, “Microwatt Computing – Application-Driven Architectures for Wireless Sensor Devices,” 2007

Semiconductor Research Association SoC Design Challenge, 1st Prize Award in Phase 2 includes cash prize and design fabrication on IBM .18um process (submission co-lead with Gu-Yeon Wei), 2006.

Catalyst Foundation, “ $\mu$ Watt Computing - Application-Driven Circuits and Architectures for Wireless Sensor Devices,” 2005-06.

National Science Foundation, Principal Investigator, CCF-0448313, “CAREER: A Framework for Early-Stage Computer Architecture Design Space Exploration and Optimization,” 2005–2010.

National Science Foundation, Principal Investigator (co-PIs are Gu-Yeon Wei and Michael Smith), CCF-0429782, “An adaptive alarm-based approach to high-performance/low-cost computing”, 2004–2007.

Intel Research Gift, Principal Investigator, “Thermal-Aware Microprocessor Design: Studying the Impact of Advanced Cooling Technologies on Chip Floorplans and Microarchitecture,” 2004–2007.

IBM Faculty Partnership Award, 2003–05.

National Science Foundation, co-PI (PI is Margo Seltzer, other co-PIs are Wei, Kung, Tarokh), SCI-0330244, “SENSORS: Hourglass: An Infrastructure for Sensor Network”, 2003–2007.

## UNIVERSITY TEACHING

Harvard University. Computer Science 141: Computing Hardware. Digital Logic Design and Basic Computer Architecture. Fall 2005, Fall 2006, Fall 2007.

Harvard University. Computer Science 146: Computer Architecture. Introduction to Quantitative Approach to Computer Architecture. Fall 2002, Spring 2004, Spring 2005.

Harvard University. Computer Science 246: Advanced Computer Architecture. Power-aware Computer Systems Graduate Course and Design Projects. Spring 2003, Fall 2003, Fall 2004, Spring 2006, Spring 2007.

## CONFERENCE ORGANIZATION ACTIVITIES

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2008

Technical Program Committee Co-Chair, Special Issue of IEEE Micro Micro’s Top Picks from Computer Architecture Conferences, 2008.

Program Committee, International Symposium on Microarchitecture, 2007.

Program Committee, International Symposium on Low Power Electronics and Design, 2007.

Publication Chair and Program Committee, International Symposium on Performance Analysis of Systems and Software, 2007.

Program Vice-Chair, and Program Committee, Technology-driven Architectures, ACM International Conference on Computing Frontiers, 2007.

Program Committee, Special Issue of IEEE Micro Micro's Top Picks from Computer Architecture Conferences, 2007.

Program Committee, International Symposium on High-Performance Computer Architecture, 2007.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2007.

Program Committee, International Conference on Architectural Support for Programming Languages and Operating Systems, 2006.

Track Co-chair (with Michael Gschwind), Processor Architecture Track, International Conference on Computer Design, 2006.

Program Committee, International Symposium on High-Performance Computer Architecture, 2006.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2006.

Program Committee, International Parallel and Distributed Processing Symposium, 2006.

Program Committee, International Conference on Parallel and Distributed Systems, 2006.

Track Co-chair (with Michael Gschwind), Processor Architecture Track, International Conference on Computer Design, 2005.

Program Committee, International Symposium on Low Power Electronics and Design, 2005.

Program Committee, International Conference on Computer Design, 2004.

Registration and Finance Chair, International Symposium on Microarchitecture, 2004.

Program Committee, International Symposium on Low Power Electronics and Design, 2004.

Program Committee, International Conference on Computer Design, 2003.

Program Committee, International Symposium on High-Performance Computer Architecture, 2003.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2002.

Program Committee, International Symposium on Performance Analysis of Systems and Software, 2001.

Web and Publicity Co-Chair, International Symposium on Performance Analysis of Systems and Software, 2001.