Research Statement

David Brooks

As a computer architect, it is exciting to see the rapidly expanding interest in power-aware computing at the architectural and software level. Power-aware computing has traditionally been the primary focus of designers of portable and battery-powered computing systems and has in the past largely been considered a low-level circuit design issue. In the past several years, we have seen two major shifts in the focus of power-aware computing that have greatly increased the amount of research interest in this field. First, the need for power-efficient designs is no longer solely associated with portable computing systems. Power dissipation has rapidly become a first-order design constraint in virtually every type of computing system including hand-held devices, set-top entertainment systems, desktop computers, and the most performance-hungry compute servers. The second major shift is that researchers in power-aware design have begun to focus on power and energy savings at higher levels in the design hierarchy including the logic design, microarchitecture, instruction set architecture, and software.

These two major shifts have greatly increased the amount of research interest and the potential for reducing power and energy consumptions in computer systems. However, when we consider the importance of power-aware computing in more complex systems, as well as power savings techniques at the architectural and software levels, power modeling becomes a significant challenge. Because of this, my thesis research at Princeton has had two major thrusts:

- First, I have addressed the problem of architectural-level power modeling by developing a framework for estimating power on top of an architectural performance simulator. This framework, called Wattch, is publicly available for the research community to develop and use.
- Second, my research has utilized this framework to develop techniques for reducing power in high-performance computing systems.

Architectural-level Power Modeling

Estimating the power dissipation of a computing system generally requires transistor-level circuit schematics and a detailed circuit simulation environment such as SPICE. This poses two major problems for modeling power at the architectural level. First, circuit-level simulation is extremely slow, requiring several orders of magnitude more time per instruction than architectural-level performance simulation. Second, architectural level studies are generally performed in the planning stages of the design before the circuit and RTL design has begun to take place.

To overcome these problems, intelligent abstractions must be developed. In my research, I developed analytical power models for common hardware structures that are present in most microprocessors. These structures include register files, caches, content-associative memories, and interconnect. These power models are parameterizable allowing structures with various sizes and attributes to be instantiated. Finally, the power models are tightly integrated into a traditional architectural-level performance simulator. Cycle-level activity and utilization statistics from the performance simulator are combined with the power models of the hardware structures to provide power estimates. This framework provides accurate power estimates on a per-cycle basis with approximately a 30% simulation time overhead over performance simulation alone. My research has also focused on the validation of this framework and will continue to do so as improvements are made to this modeling methodology. Establishing a solid power modeling methodology is critical for allowing architects to rapidly explore large design spaces and to consider methods to reduce power dissipation in the planning stage of the design.
Techniques for Power-Aware Design

The goal of developing accurate and efficient power modeling methodologies is to assist in the development of techniques for power-efficient design. In my thesis research at Princeton, I developed several techniques including value-based clock gating and dynamic thermal management. Value-based clock gating seeks to disable the upper portion of functional units based on dynamic information gathered about the values being executed. This technique capitalizes on the disparity between the bitwidth requirements of address calculation and computation calculations. This disparity increases when considering processors with wide datapaths, and we demonstrated that in 64-bit processors this technique can reduce the power dissipation of the functional units by over 50%, which can lead to full chip power savings of roughly 5-10%. During my internship at Intel, I investigated practical implementations of this technique as well extensions into the memory hierarchy.

More recently, I have investigated the benefits of dynamic thermal management. This is a method to reduce the cost of thermal packaging of microprocessors by reducing the effective maximum power dissipation of the processor. This technique is based on the observation that the maximum chip power dissipation is achieved only under extreme circumstances that do not typically occur in typical applications. With the use of on-chip thermal sensors, the operating system or microarchitecture can use various techniques to dynamically trade small amounts of performance for reduced power dissipation when these unusual circumstances occur. We demonstrated that for many applications the thermal packaging requirements can be reduced substantially while maintaining performance.

Future Directions

In my future research I would like to continue to pursue opportunities in the two areas that I conducted my thesis research as well as to look at the design of emerging architectures in which power is a key design constraint. In the area of high-level power modeling, there is a definite need to continue to develop abstractions to model power at the architectural and software level. For example, at the operating system level, power estimation could be performed through the use of on-chip performance counters, possibly including the addition of counters to enable more accurate power estimates. At the compiler level, power models could be integrated into a compiler infrastructure to statically estimate the power of code sequences. As an example, in statically scheduled architectures, the compiler has detailed knowledge about when instructions will be executing. Combining this information with power models of the hardware structures in the microprocessor would enable compiler-level power estimation. This modeling research is essential to enable the development of power saving techniques at the software level.

I also see many opportunities for research in developing techniques for power-aware design. I intend to continue to explore the dynamic nature of program execution to identify areas for power savings at the hardware-software interface. For example, there is a significant opportunity for power savings by performing optimizations on the dynamic instruction stream. These optimizations have begun to be proposed for performance, but similar as well as new techniques can have an even more significant impact on power.

In a more general sense, I am interested in applying my experience in power-efficient design to novel classes of architectures. As PDAs and other non-traditional mobile computing systems increase in popularity, the architecture and system design of these devices will have to meet growing performance demands without increasing the energy requirements of current systems. Network processors also represent a burgeoning area of interest for computer architects, as they require large amounts of processing capability within tight power budgets. Power must be minimized because network equipment manufacturers will eventually integrate tens or hundreds of these network processors into a single switch or router.

An important part of my future research will be strong interaction with partners in industry. The ultimate goal of research in computer systems is to generate ideas, tools, and methodologies that can eventually be used in real systems. Pursuing a research idea from initial conception through industrial acceptance as I did in my research in value-based clock gating at Intel is personally rewarding. Furthermore, interactions with industry are important for acquiring resources and knowledge that is essential for research in this field.
Teaching Statement

David Brooks

I enjoy teaching and would feel comfortable teaching courses in computer architecture, digital logic and design, VLSI circuits, and compiler design. At Princeton, I was the teaching assistant for a senior and first-year graduate student VLSI design course during the spring of 2000 with Professor Jonathan Babb. During this TA assignment I assisted in the design of the homework and lab assignments as well as the course project, and I was responsible for installing and maintaining the CAD tools. I was also given the opportunity to give lectures to the class when Professor Babb was out of town. This assistantship gave me the opportunity to see both the challenges and rewards of the teaching experience, and the feedback from the students was extremely helpful. Through the weekly Q&A office hours, I realized that teaching was more than the knowledge of the subject that a teacher has, but also the ability to explain the concepts in simple words yet encourage students to think and learn.

When designing coursework for my own classes, I will primarily concentrate on enriching the learning experience with hands-on labs and projects. The subject of computer architecture, my most familiar teaching subject, has the benefit of excellent textbooks at both the introductory and advanced level, particularly the well-known Hennessey and Patterson series. While these texts provide a solid foundation for the basic material in this field, it is crucial to supplement this material with appropriate labs and projects. My goal in devising these projects will be to reinforce the material learned in the textbook and the class, while giving the students the practical experience that they will need in industry or as a graduate student. My background in architectural tool development and hardware design gained during my graduate studies at Princeton and during my internships at Intel and IBM has given me some of the insight that is necessary to design interesting and relevant course projects.

Besides traditional classroom oriented instruction, I look forward to working with motivated undergraduate students on independent research projects. Being able to work with faculty on cutting edge research problems is one of the primary benefits for undergraduates at research universities, and they should be encouraged to participate in this whenever possible. My independent research projects were the highlight of my undergraduate career at the University of Southern California and motivated me to pursue a PhD degree at Princeton.

I look forward to being a teacher and providing guidance for the younger generations to explore the possibilities of the ever evolving computer era. Through my school years, I’ve benefited from the advice my teachers have given me, and I am deeply grateful for the patience and perspectives that they shared with me. I am committed to doing the same for my students in my career.