

# Alexandra FEDOROVA

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## RESEARCH INTERESTS:

SYSTEMS – Operating system scheduling for chip multiprocessors and multithreaded processors, performance evaluation, performance modeling and cache modeling on chip multiprocessors, transactional memory

## EDUCATION:

**2000-2006**      **Ph.D. in Computer Science, *Harvard University, Cambridge, MA, USA***

*Thesis title:* Operating System Scheduling for Chip Multithreaded Processors

*Thesis advisor:* Margo Seltzer

*Degree granted:* November 7, 2006

**2000-2002**      **M.S. in Computer Science, *Harvard University, Cambridge, MA, USA***

**1997-1999**      **B.A. in Computer Science and Economics, *Smith College, Northampton, MA, USA***

- Cum Laude
- GPA: 3.87
- GPA in Computer Science major: 4.0

**1996-1997**      **Exchange student, *Pomona College, CA, USA***

- Selected out of a large pool of international applications to participate in the exchange program sponsored by the United States Information Agency

**1994-1996**      **International University of Moscow, B.A. in Economics candidate, *Russia***

- GPA: 95.6 out of 100

## WORK EXPERIENCE:

**From**              **Assistant Professor, *Simon Fraser University, Vancouver, Canada***

**December 2006**      • Tenure-track assistant professor position at a research university

**2000-2006**      **Research assistant, *Harvard University, Cambridge, MA***

- Explore issues in operating system design for chip multithreaded processors
- Model performance of CPU caches in chip multithreaded processors
- Study application performance on the direct-access file system (DAFS)

**2004-2006**      **Research intern, Scalable Synchronization Group  
*Sun Microsystems Laboratories, Burlington, MA, USA***

- Study performance and usability of the Hybrid Transactional Memory system

**2003-2004**      **Research intern, Iceberg Group  
*Sun Microsystems Laboratories, Burlington, MA, USA***

- Analyzed performance of applications on chip multithreaded processors
- Designed and implemented a new operating system scheduler for multithreaded

chip multiprocessors in Solaris™ 10

- Participated in the implementation and validation of Sun Niagara® processor hardware simulator
- Published ten internal technical reports
- Lead inventor on seven patent applications

**1999-2000**     **Software engineer, EMC Corporation, Westboro, MA, USA**

- Designed and developed server management software for the Windows platform
- Received only “Exceeds expectations” or “Excels” marks during the annual performance review

**Summer 1998**     **Research assistant, Smith College, Northampton, MA, USA**

- Worked on a Video-On-Demand (VoD) project
- Designed a software substrate for running VoD services

#### **ADDITIONAL TEACHING EXPERIENCE:**

**Fall 2005**     **Teaching assistant for *Advanced Operating Systems, Harvard University***

- Assisted students with final research projects
- Facilitated technical discussions of the assigned readings

**Spring 2002,**     **Teaching assistant for *Introduction to Operating Systems, Harvard University***

**Spring 2003**

- Designed and taught supplementary course sections for groups of 6-8 students
- Worked with groups of students to review their design specifications and code
- Held regular office hours in the lab, helped students with online debugging
- Graded assignments and participated in the design of assignments
- Managed the course at the Harvard Extension School
- Taught sections that were video-recorded for distance-education students

**January 1999**     **Winter term teacher, Smith College, Northampton, MA, USA**

- Designed and taught *Introduction to Computers and the Internet* to a class of 15 students.

#### **PUBLICATIONS:**

##### **Thesis:**

Alexandra Fedorova. Operating System Scheduling for Chip Multithreaded Processors, *Harvard University*, September 2006

##### **Refereed papers:**

Peter Damron, Alexandra Fedorova, Yosef Lev, Victor Luchangco, Mark Moir and Daniel Nussbaum. Hybrid Transactional Memory. To appear in *Proceedings of the Twelfth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, October 2006

Alexandra Fedorova, Margo Seltzer, and Michael D. Smith. A Non-Work-Conserving Operating System Scheduler for SMT Processors. In *Proceedings of the Workshop on the Interaction between the Operating Systems and Computer Architecture (WIOSCA)*, in conjunction with ISCA-33, Boston, MA, June 2006

Aaron B. Brown, Anupam Chanda, Rik Farrow, Alexandra Fedorova, Petros Maniatis, and Michael L. Scott. The Many Faces of Systems Research - and How to Evaluate Them. In *Proceedings of HotOS X, Tenth Workshop on Hot Topics in Operating Systems* Santa Fe, NM, June 2005

Alexandra Fedorova, Margo Seltzer, Christopher Small and Daniel Nussbaum. Performance Of Multithreaded Chip Multiprocessors And Implications For Operating System Design. In *Proceedings of the USENIX 2005 Annual Technical Conference*, Anaheim, CA, April 2005

Alexandra Fedorova, Christopher Small, Daniel Nussbaum and Margo Seltzer. Chip Multithreading Systems Need a New Operating System Scheduler. In *Proceedings of 11th ACM SIGOPS European Workshop*, Leuven, Belgium, September 2004

Alexandra Fedorova, Margo Seltzer, Kostas Magoutis, and Salimah Addetia. Application Performance on the Direct Access File System. In *Proceedings of Workshop on Software and Performance 2004 (WOSP'04)*, Redwood City, CA, January 14-16, 2004

Kostas Magoutis, Salimah Addetia, Alexandra Fedorova, Margo I. Seltzer. Making the Most out of Direct Access Network-Attached Storage. In *Proceedings of Second USENIX Conference on File and Storage Technologies (FAST'03)*, San Francisco, CA, March 31-April 2, 2003

Kostas Magoutis, Salimah Addetia, Alexandra Fedorova, Margo I. Seltzer, Jeffrey S. Chase, Andrew J. Gallatin, Richard Kisley, Rajiv G. Wickremesinghe, Eran Gabber. Structure and Performance of the Direct Access File System. In *Proceedings of the USENIX Annual Technical Conference*, Monterey, CA, June 9-14, 2002. Best paper award

#### **Patents:**

Alexandra Fedorova, An Operating System Method To Achieve Fair Cache Sharing On Chip Multiprocessors, *US Patent Application, filed by Sun Microsystems Laboratories*, 2006

Alexandra Fedorova, Modeling How Multithreaded Processors Hide Individual Threads' Memory Latency, *US Patent Application, filed by Sun Microsystems Laboratories*, 2005

Alexandra Fedorova, Modeling Memory-Bus Delays In Multithreaded, Chip Multithreaded Or Multiprocessor Systems, *US Patent Application Filed by Sun Microsystems Laboratories*, 2005

Alexandra Fedorova and Christopher Small, Method And Apparatus For Scheduling Threads On Multithreaded, Multicore And Chip-Multithreaded Processors Based On Their Estimated L2 Miss Rates, *US Patent Application, filed by Sun Microsystems Laboratories*, 2005

Alexandra Fedorova and Christopher Small, Method And Apparatus For Efficient Online Estimation Of L2 Miss Rate For Groups Of Threads Sharing The L2 Cache, *US Patent Application, filed by Sun Microsystems Laboratories*, 2005

Alexandra Fedorova, Christopher Small and Daniel Nussbaum, Cache-Conscious Scheduling Using Balance-Sets For CMT, *US Patent Application, filed by Sun Microsystems Laboratories*, 2004

Christopher Small, Alexandra Fedorova, Daniel Nussbaum, Techniques For Thread Scheduling On CMT Processors, *US Patent Application, filed by Sun Microsystems Laboratories*, 2004

## **Technical Reports:**

Alexandra Fedorova, Margo Seltzer, and Michael D. Smith, Cache-Fair Thread Scheduling for Multicore Processors, *Technical Report TR-17-06, Division of Engineering and Applied Sciences, Harvard University*, October 2006

Alexandra Fedorova, Margo Seltzer and Mike Smith. Modeling Effects of Memory Hierarchy Performance on Throughput of Multithreaded Processors. *Technical Report TR-15-05, Division of Engineering and Applied Sciences, Harvard University*, June 2005

Alexandra Fedorova, Margo Seltzer, Christopher Small and Daniel Nussbaum. Throughput-Oriented Scheduling On Chip Multithreading Systems. *Technical Report TR-17-04, Division of Engineering and Applied Sciences, Harvard University*, August 2004

Daniel Nussbaum, Alexandra Fedorova and Christopher Small. An overview of the Sam CMT simulator kit. *Technical Report TR-2004-133, Sun Microsystems Research Labs*, March 2004

Joseph O'Rourke and The Smith College Problem Solving Group (including A.Fedorova), PushPush is NP-hard in 3D. *Smith College Technical Report 064*, November 1999

## **TALKS:**

Cache-fair Scheduling for Chip Multithreaded Processors, VMWare, San Jose, September 1, 2006

A Non-Work-Conserving Scheduler for Simultaneous Multithreading Processors, Workshop on the Interaction between Operating Systems and Computer Architecture, Boston, June 18, 2006

Operating System Scheduling for Multicore Processors, Intel, Santa Clara, May 11, 2006

Cache-fair Thread Scheduling for Multicore Processors, Sun Microsystems Laboratories Seminar Series, February 3, 2006

Operating System Methods For Improved Resource Sharing On Chip Multiprocessors. Harvard Industrial Partnership Symposium, October 21, 2005

A High-Performance Cache Model. Cider Seminar, University of Toronto, Canada, June 21, 2005

Operating System Scheduling for Chip Multithreaded Processors. Sun Microsystems, Burlington, MA, June 6, 2005

Performance of Chip Multithreaded Processors and Implications for Operating System Design. USENIX Annual Technical Conference, Anaheim, CA, April 14, 2005

Implementing an Operating System Scheduler for Multithreaded Chip Multiprocessors. Work-in-progress session, 6<sup>th</sup> Symposium on Operating Systems Design and Implementation (OSDI 2004), December 8, 2004

Throughput-Oriented Scheduling on Chip Multithreading Systems, Performance Strategic Working Group, Sun Microsystems, Burlington, MA, September 2, 2004

Chip Multithreading Systems Need a New Operating System Scheduler. SIGOPS European Workshop, Leuven, Belgium, September 20, 2004

Application Performance on the Direct Access File System. Workshop on Software and Performance (WOSP 2004), Redwood City, CA, January 15, 2004

Using a Vector-Based Approach For Modeling Performance of Distributed Systems. Work-in-progress session. 2<sup>nd</sup> USENIX Conference on File Access and Storage Technologies (FAST 2003), San Francisco, CA, April 1, 2003

### **PROFESSIONAL SERVICE:**

- Served as an external reviewer for the following conferences:
  - 7<sup>th</sup> Symposium on Operating System Design and Implementation (OSDI 2006)
  - 20<sup>th</sup> International Symposium on Distributed Computing (DISC 2006)
  - 26<sup>th</sup> International Conference on Distributed Computing Systems (ICDCS 2006)
  - IEEE International Parallel and Distributed Processing Symposium (IPDPS 2006)
  - 10<sup>th</sup> Workshop on Hot Topics on Operating Systems (HotOS 2005)
  - 6<sup>th</sup> Symposium on Operating Systems Design and Implementation (OSDI 2004)
  - 9<sup>th</sup> Workshop on Hot Topics on Operating Systems (HotOS 2003)
  - USENIX Annual Technical Conference, 2003
- Served as a scribe at the 10<sup>th</sup> Workshop on Hot Topics on Operating Systems (HotOS 2005)
- Organized and conducted a series of lectures *How to survive graduate school* for Ph.D. students in the Computer Science department at Harvard University, 2003-2004
- Organized and conducted an introductory Q&A session for prospective graduate students in the Computer Science department at Harvard University, 2004

### **HONORS AND AWARDS:**

- 2002: Best paper award at the USENIX Annual Technical Conference
- 1999: Bert Mendelson Prize for excellence in Computer Science, Smith College, USA
- 1997-1999: Dean's List in every semester, Smith College, USA
- 1998: ACM Student Research Contest Finalist
- 1998: Schultz Research Fellowship recipient
- 1996: United States Information Agency exchange program grant recipient
- 1995-1996: Recipient of the merit-based grant for full tuition, International University of Moscow