CURRICULUM VITAE ET STUDIORUM

Simone Campanoni

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Personal Information

Birthdate: April 30th, 1981
Birthplace: Tradate, Italy
Italian Nationality
US green card holder
Native language: Italian
Foreign languages: English

Current Position

Position Research Associate in the School of Engineering and Applied Sciences at Harvard University.

Period From November 2012.

BIOGRAPHY

Simone Campanoni is a research associate in the School of Engineering and Applied Sciences at Harvard University working with Profs. Gu-Yeon Wei and David Brooks. Simone's main research area is **compilers**. His research focuses on code compilation challenges, such as optimization for both power efficiency and performance. Simone addresses these challenges through **codesign** of compilers and the hardware platforms they target. His research on compilers has enhanced both compile-time and run-time efficiency.

Simone's current work uses static and dynamic compilation, run-time optimization, and advanced code analysis to extract coarse-grained parallelism for many-core architectures from general purpose sequential code. He is the author of HELIX, a research project demonstrating these code transformations.

Simone received his Ph.D. degree with highest honors from Politecnico di Milano University in 2009. He is the author of ILDJIT, a parallel compilation framework demonstrating principles from his dissertation. ILDJIT includes both static and dynamic compilers. It is used on several research projects to investigate new approaches to program introspection, optimization, and micro-architectural design.

RESEARCH INTERESTS

Parallelizing Sequential Code

The multicore revolution in microprocessor architecture has left most programs behind. A program that maps easily to multicore architectures is the exception, not the rule. I am interested in showing multiple ways to parallelize the others (e.g., common, sequentially-designed programs) for modern and next-generation architectures.

The HELIX research project demonstrates the potential of leveraging low latency communication links among cores within a single chip to efficiently run parallelized code. The HELIX compiler demonstrates this potential on today's commodity processors by automatically speeding up sequential programs previously thought not to be parallelizable. The HELIX-RC compiler/architecture co-design highlights the benefits of including hardware support for a proactive, cache-based, low-latency core-to-core interconnect. Finally, HELIX-UP, shows the value of coupling the approximate computing paradigm with the parallelization performed by the HELIX compiler.

Compiling for Resilient Architecture

Safety margins in conventional architectures are conservative to *always* avoid computational errors leading to energy inefficiencies. Resilient architectures squeeze these margins to save energy, correcting errors through costly rollback. Co-designed compilers can help resilient architectures to reduce their overhead by adapting the running code to their run-time characteristics.

For example, in our ALARM compiler, a resilient architecture propagates information about run-time rollback up to the co-designed compiler, which dynamically adapts the code to reduce the likelihood of further roll-back.

Bytecode Virtual Machines

Virtual machines designed to execute bytecode programs are everywhere. The most successful and widely-adopted examples are Java and .NET. Browsers are virtual machines as well thanks to their ability to run programs written in multiple languages (e.g., JavaScript).

A bytecode virtual machine usually includes several components. Code generators, code optimizers, garbage collectors, execution engine, and profilers are the most common ones. Understanding interactions of these components allows them to be co-designed, which open interesting optimization opportunities. To enable these studies, we built the open source ILDJIT compilation framework.

An example of these optimizations is the dynamic look-ahead (DLA). In DLA, code generators and optimizers are driven by feedback coming from the execution engine to suppress dynamic compilation latency.

PUBLICATIONS

Selected Publications

1. Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks. "HELIX-UP: Relaxing Program Semantics to Unleash Parallelization". 12th International Symposium on Code Generation and Optimization (**CGO**), San Francisco, California, USA. February 7-11, 2015. Acceptance rate: 27.3% (24/88). One of four papers nominated for the Best Paper Award by the Program Committee. Acceptance rate of nominated papers: 4.6% (4/88). Download

2. Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs". In proceedings of the 41st International Symposium on Computer Architecture (**ISCA**), Minneapolis, Minnesota, USA, June 14-18, 2014. Acceptance rate: 17.8% (46/258). This is one of the three papers nominated by the program committee for CACM research highlight. Acceptance rate of nominated papers: 1.2% (3/258). Download

3. Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks. "HELIX: Making the Extraction of Thread-Level Parallelism Mainstream". **IEEE Micro**, 12 June 2012. IEEE computer Society Digital Library. IEEE Computer Society. Download

Awards

1. HiPEAC award: Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs". International Symposium on Computer Architecture (ISCA), 2014.

2. HiPEAC award: Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks. "The HELIX Project: Overview and Directions". Design Automation Conference (DAC), 2012.

3. HiPEAC award: Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto and Marco D. Santambrogio. "Metronome: Operating System Level Performance Management via Self-Adaptive Computing". Design Automation Conference (DAC), 2012.

4. IEEE Top Picks: Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise in Production Processors". IEEE Micro's Top Picks in Computer Architecture Conferences. January, 2011.

5. Best paper: Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". PhDay at Politecnico di Milano, 2008.

6. Ph.D. with the highest honors: Simone Campanoni. "Dynamic Compilation and Parallelism: Theory and large scale experimentation". Politecnico di Milano, 3 March 2010.

Books

1. Simone Campanoni. "Guide to ILDJIT". Springer. 1st Edition. September 2011. ISBN: 978-1-4471-2193-0.

International Conferences

2. Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks. "HELIX-UP: Relaxing Program Semantics to Unleash Parallelization". It will appear at the 12th International Symposium on Code Generation and Optimization (**CGO**), San Francisco, California, USA. February 7-11, 2015. Acceptance rate:

27.3% (24/88). One of four papers nominated for the Best Paper Award by the Program Committee. Acceptance rate of nominated papers: 4.6% (4/88).

3. Simone Campanoni, Kevin Brownell, Svilen Kanev, Timothy M. Jones, Gu-Yeon Wei and David Brooks. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs". In proceedings of the 41st International Symposium on Computer Architecture (**ISCA**), Minneapolis, Minnesota, USA, June 14-18, 2014. Acceptance rate: 17.8% (46/258). This is one of the three papers nominated by the program committee for CACM research highlight. Acceptance rate of nominated papers: 1.2% (3/258).

4. Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks. "The HELIX Project: Overview and Directions". In proceedings of the 48th Design Automation Conference (**DAC**), San Francisco, California, USA, June 3-7, 2012. Invited paper.

5. Filippo Sironi, Davide B. Bartolini, Simone Campanoni, Fabio Cancare, Henry Hoffmann, Donatella Sciuto and Marco D. Santambrogio. "Metronome: Operating System Level Performance Management via Self-Adaptive Computing". In proceedings of the 48th Design Automation Conference (**DAC**), San Francisco, California, USA, June 3-7, 2012. Acceptance rate: 22.7% (168/741).

6. Simone Campanoni, Timothy M. Jones, Glenn Holloway, Vijay Janapa Reddi, Gu-Yeon Wei and David Brooks. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing". In proceeding of 10th International Symposium on Code Generation and Optimization (**CGO**), San Jose, California, USA, March 31st - April 4th, 2012. Acceptance rate: 28.9% (26/90).

7. Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Smoothing: Characterizing and Mitigating Voltage Noise in Production Processors via Software-guided Thread Scheduling". In proceedings of 43rd International Symposium on Microarchitecture (**MICRO**), Atlanta, Georgia, USA, December 4-8, 2010. Acceptance rate: 18.1% (45/248).

8. Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Software-Assisted Hardware Reliability: Abstracting Circuit-level Challenges to the Software Stack". In proceedings of IEEE 2009 46th International Conference on Design Automation Conference (**DAC**), San Francisco, July 26-31, 2009. Acceptance rate: 21.7% (148/682).

9. Simone Campanoni and Stefano Crespi Reghizzi. "Traces of control-flow graphs". In proceedings of 13th International Conference on Developments in Language Theory (**DLT**), Stuttgart University, Germany, June 30 - July 3, 2009. Acceptance rate: 45.7% (32/70).

10. Simone Campanoni, Martino Sykora, Giovanni Agosta and Stefano Crespi Reghizzi. "Dynamic Look Ahead Compilation: a technique to hide JIT compilation latencies in multicore environment". In proceedings of 18th International Conference on Compiler Construction (**CC**), York, United Kingdom, March 22-29, 2009. Acceptance rate: 25% (18/72).

11. Simone Campanoni and William Fornaciari. "Node-Level Optimization of Wireless Sensor Networks". In proceedings of IEEE 2008 Wireless Communications, Networking and Mobile Computing (**WiCOM**), Dalian, China, October 12-14, 2008.

12. Simone Campanoni and William Fornaciari. "Models and Tradeoffs in WSN System-Level Design". In proceedings of IEEE 2008 International Conference on Digital System Design (**DSD**), Parma, Italy, September 3-5, 2008. Acceptance rate: 26%.

13. Simone Campanoni and William Fornaciari. "Multi-level Design and Optimization of Wireless Sensor Networks". In proceedings of IEEE 2008 International Conference on Networked Sensing Systems (**INSS**), Kanazawa, Japan, June 17-19, 2008.

14. Simone Campanoni and William Fornaciari. "Ensuring Feasibility of Wireless Sensor Networks". In proceedings of IEEE 2008 International Conference on Circuits and Systems for Communications (**ICCSC**), Shanghai, China, May 26-28, 2008.

15. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "ILDJIT: a parallel dynamic compiler". In proceedings of 16th IFIP/IEEE International Conference on Very Large Scale Integration (**VLSI-SoC**), Rhodes Island, Greece, October 13-15, 2008.

16. Simone Campanoni and William Fornaciari. "SWORDFISH: a Framework to Formally Design WSNs Capturing Events". In proceedings of IEEE 2007 International Conference on Software, Telecommunications and Computer Networks (**SoftCOM**), Split-Dubrovnik, Croatia, September 27-29, 2007.

Magazines

17. Simone Campanoni, Timothy M. Jones, Glenn Holloway, Gu-Yeon Wei and David Brooks. "HELIX: Making the Extraction of Thread-Level Parallelism Mainstream". **IEEE Micro**, 12 June 2012. IEEE computer Society Digital Library. IEEE Computer Society.

18. Vijay Janapa Reddi, Svilen Kanev, Wonyoung Kim, Simone Campanoni, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise in Production Processors". **IEEE Micro**'s Top Picks in Computer Architecture Conferences. Vol. 3, no. 1, 2011.

International Journals

19. Vijay Janapa Reddi, Simone Campanoni, Meeta S. Gupta, Kim Hazelwood, Michael D. Smith, Gu-Yeon Wei, and David Brooks. "Eliminating Voltage Emergencies via Software-Guided Code Transformations". ACM Transactions on Architecture and Code Optimization (**TACO**). Vol. 7, no. 2, 2010.

20. Simone Campanoni, Giovanni Agosta, Stefano Crespi Reghizzi and Andrea Di Biagio. "A highly flexible, parallel virtual machine: design and experience of ILDJIT". Software: Practice and Experience (**SPE**). Vol. 40, no. 2, 2010.

Book Chapters

21. Marcello Mura, Simone Campanoni, William Fornaciari, Mariagiovanna Sami. "Optimal Design of Wireless Sensor Networks". Chapter 19 of "Methodologies and Technologies for Networked Enterprises", in Lecture Notes in Computer Science, Vol. 7200, Anastasi, G.; Bellini, E.; Di Nitto, E.; Ghezzi, C.; Tanca, L.; Zimeo, E. (Eds.), 2012, ISBN 978-3-642-31738-5, July 2012.

International Workshops

22. Niall Murphy, Timothy M. Jones, Simone Campanoni, Robert Mullins. "Limits of Static Dependence Analysis for Automatic Parallelization". 18th International Workshop on Compilers for Parallel Computing (**CPC**). London, UK. January 7-9, 2015.

23. Simone Campanoni, Svilen Kanev, Kevin Brownell, Gu-Yeon Wei and David Brooks. "Breaking Cyclic-Multithreading Parallelization with XML Parsing". In proceedings of the 2nd International Workshop on Parallelism in Mobile Platforms (**PRISM**). Minneapolis, Minnesota, USA, June 14, 2014.

24. Simone Campanoni and Luca Rocchini. "Static Memory Management within Bytecode Languages on Multicore Systems". In proceedings of Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (**CHANGE**). Newport Beach, California, March 6, 2011.

25. Michele Tartara, Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "Parallelism and Retargetability in the ILDJIT Dynamic Compiler". In proceedings of Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (**PARMA-DITAM**). Hannover, Germany, February 22th, 2010.

26. Michele Tartara, Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "Just-In-Time compilation on ARM processors". In proceedings of ACM 4th Workshop on the Implementation, Compilation, Optimization of Object-Oriented Languages, Programs and Systems (**ICOOOLPS**). Genova, Italy, July 6th, 2009.

27. Vijay Janapa Reddi, Meeta S. Gupta, Krishna K. Rangan, Simone Campanoni, Glenn Holloway, Michael D. Smith, Gu-Yeon Wei and David Brooks. "Voltage Noise: Why It's Bad, and What To Do About It". In proceedings of IEEE 2009 5th Workshop on Silicon Errors in Logic - System Effects (**SELSE**), Stanford University, March 24th and 25th, 2009.

28. Stefano Crespi Reghizzi and Simone Campanoni. "Traces of control-flow graphs". ESF Workshop on Developments and New Tracks in Trace Theory, Cremona, Italy, 9-11 October 2008.

Italian National Conferences

29. Simone Campanoni, Michele Tartara, and Stefano Crespi Reghizzi. "ILDJIT: A parallel, free software and highly flexible Dynamic Compiler". IV Conferenza Italiana sul Software Libero. Cagliari, Italy, 11 - 12 June 2010.

30. Michele Tartara, Stefano Crespi Reghizzi and Simone Campanoni. "Extending hammocks for parallelism detection". Italian Conference on Theoretical Computer Science (ICTCS). Camerino, Italy, 15 - 17 September 2010.

31. Simone Campanoni. "Parallelism on compilation and execution". PhDay at Politecnico di Milano, Milan, Italy, June 24, 2009.

32. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". PhDay at Politecnico di Milano, Best paper, Milan, Italy, June 26, 2008.

Posters

33. Simone Campanoni, Glenn Holloway, Gu-Yeon Wei, and David Brooks. "Relaxing Program Semantics to Unleash Parallelization". In the Center for Future Architectures Research (C-FAR). November 2014.

34. Michael Lyons, Judson Porter, Yakun Sophia Shao, Simone Campanoni, David Brooks. "Architecture Design for Fine-grained Hardware Acceleration". In The Gigascale Systems Research Center(GSRC) Annual Symposium, September 2010.

35. Simone Campanoni. "Dynamic Compilation and Parallelism. Theory and Large Scale Experimentation". PhDay at Politecnico di Milano, Milan, Italy, June 26, 2009.

36. Simone Campanoni. "ILDJIT: Intermediate Language Distributed Just In Time". PhDay at Politecnico di Milano, Milan, Italy, June 24, 2009.

Theses

1. Simone Campanoni. "Dynamic Compilation and Parallelism: Theory and large scale experimentation". PhD Dissertation, December 2009.

2. Simone Campanoni. "Intermediate Language Distributed Just In Time for the CIL Bytecode". Master Thesis, July 2006.

3. Simone Campanoni. "Ontology Packet Manager". Bachelor Thesis, July 2004.

Technical Reports

4. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". SIGPLAN Notices, Volume 43, Number 4, April, 2008.

5. Simone Campanoni and William Fornaciari. "Design and optimization of Wireless Sensor Networks". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 17, Anno 2008.

6. Simone Campanoni, Giovanni Agosta and Stefano Crespi Reghizzi. "A parallel dynamic compiler for CIL bytecode". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 3, Anno 2008.

7. Simone Campanoni and William Fornaciari. "Board-Level clustering of sensor network nodes". Politecnico di Milano, Dipartimento di Elettronica, Technical Report n. 61, Anno 2007.

Tutorials

1. "Hands-On ILDJIT 2.0 for Static and Dynamic Program Analysis and Transformation". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with the 12th ISPA Conference). Milan, Italy. August 29th, 2014. Full day tutorial.

2. "ILDJIT: Hands-On ILDJIT for Static and Dynamic Program Analysis and Transformation". Presented at International Symposium on Code Generation and Optimization (CGO), April 2012. Full day tutorial.

3. "ILDJIT: a Compilation Framework for Static and Dynamic Program Analysis and Optimization". Presented at the 44th International Symposium on Microarchitecture (MICRO), December, 2011. Full day tutorial.

4. "ILDJIT: a compilation framework for program introspection, optimization and micro-architectural design." Presented at High-Performance and Embedded Architectures and Compilers (HiPEAC), January 2011. Half day tutorial.

5. "ILDJIT Compiler Framework for Architecture Research". Presented at the 43rd International Symposium on Microarchitecture (MICRO), December 4th, 2010. Half day tutorial.

US Patents

1. "Methods and apparatus for parallel processing". Simone Campanoni, Gu-Yeon Wei, David Brooks, Kevin Brownell, Svilen Kanev. Pending.

GRANT

January 2011 – December 2011 Microsoft Research grant with Prof. David Brooks – $20,000

December 2010 – March 2011 HiPEAC grant – €8,000

January 2007 – December 2009 ST Microelectronics grant for the PhD studies.

ACADEMIC AND PROFESSIONAL SERVICE

Program Chair

1. Program Chair with Martina Maggio and Antonio Fernndez at the 13-th IEEE "International Symposium on Parallel and Distributed Processing with Applications" (ISPA). Helsinki, Finland. August 20-22, 2015.

   Website http://research.comnet.aalto.fi/ISPA2015

2. Program Chair with Martina Maggio at the 12-th IEEE "International Symposium on Parallel and Distributed Processing with Applications" (ISPA). Milan, Italy. August 25-29, 2014.

   Website http://ispa14.necst.it

3. Program Co-Chair at the 2nd edition of the IEEE Workshop on "Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments", (co-located with DAC), San Francisco, USA, June 3, 2012.

   Website http://change.ws.dei.polimi.it

4. Vice-chairs of the track "Embedded Software and Optimization" at the 10th edition of the IEEE/IFIP "International Conference on Embedded and Ubiquitous Computing". Paphos, Cyprus. October 3-5, 2012.

Program Committee

5. Program committee of the International Symposium on Code Generation and Optimization (CGO), 2015.

6. Program committee of the DAC Workshop on Suite of Embedded Applications and Kernels (SEAK), 2014.

7. Program committee of the 7th IEEE International Symposium on Embedded Multicore Systems-on-chip (MCSoC-13). Tokyo, Japan. September 26-28, 2013.

8. Program committee at the 11th edition of the IEEE/IFIP International Conference on Embedded and Ubiquitous Computing. Zhangjiajie, China. November 13-15, 2013.

9. Program committee of the 8th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), Darmstadt, Germany, July 10-12, 2013.

10. Program committee of the 6th IEEE International Symposium on Embedded Multicore Systems-on-chip (MCSoC). Aizu-Wakamatsu, Japan. September 20-22, 2012.

11. Program committee at the special session Self-adaptable and autonomic systems at the 7th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC), York, UK, July 9-11 2012.

12. Program committee at the 9th edition of the IEEE/IFIP International Conference on Embedded and Ubiquitous Computing. Melbourne, Australia. October 24-26, 2011.

13. Program committee at the 1st edition of the IEEE Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (Change), (co-located with ASPLOS) Newport Beach, California, March 6, 2011.

14. Program committee at the 1st edition of the IEEE Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures (2 PARMA), (co-located with ARCS) Hannover, Germany, Feb 22, 2010.

Special Session Organizer

15. Organizer together with Lamia Youseff of the special session "The Future of Operating Systems for Embedded Systems and Software (ESS)" at the 50th Design Automation Conference (DAC), Austin, Texas, USA.

16. Session chair of the special session "The Future of Operating Systems for Embedded Systems and Software (ESS)" at the 50th Design Automation Conference (DAC), Austin, Texas, USA.

Journal and Magazine Reviewer

17. Reviewer of the IEEE Computer Architecture Letters 2015.

18. Reviewer of IEEE Embedded Systems Letters 2014.

19. Reviewer of the ACM Transactions on Architecture and Code Optimization (TACO) 2012, 2013, 2014.

20. Reviewer of the journal "Mobile Networks and Applications" 2013.

21. Reviewer for the following magazines: IEEE Micro 2012.

Session Chair

22. Session "Parallelism and Concurrency" at CGO 2015.

External Reviewer

23. External reviewer for the following conferences: CGO, ASPLOS, HPCA, ICS, MICRO, PACT, CCNC, IEEE Consumer Communications and Networking Conference.

TALKS

1. Simone Campanoni. "Accelerating Sequential Code with the HELIX Parallelizing Compiler". Presented at Google. Cambridge, USA. November 11th, 2014. Invited talk.

2. Simone Campanoni. "Should Compiler Designers (Re-)Focus on Extracting Parallelism?". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with ISPA). Milan, Italy. August 25th, 2014. Invited talk.

3. Simone Campanoni. "HELIX-RC: An Architecture-Compiler Co-Design for Automatic Parallelization of Irregular Programs". Presented at the 41st International Symposium on Computer Architecture (ISCA), Minneapolis, Minnesota, USA, June 16, 2014.

4. Simone Campanoni. "Breaking Cyclic-Multithreading Parallelization with XML Parsing". Presented at the 2nd International Workshop on Parallelism in Mobile Platforms (PRISM). Minneapolis, Minnesota, USA, June 14, 2014.

5. Simone Campanoni. "The HELIX Project: Goal, Status, and Potentials". Presented at ARM. Cambridge, UK. January 29th, 2014. Invited talk.

6. Simone Campanoni. "Extract Parallelism from Sequential Code for Current Commodity Multicore Processor". Presented at the workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE) (co-located with the 50th Design Automation Conference, DAC). Austin, Texas, USA. June 2nd, 2013. Invited talk.

7. Simone Campanoni. "The HELIX Project: Overview and Directions". Presented at the 48th Design Automation Conference (DAC). San Francisco, California, USA. June 5th, 2012.

8. Simone Campanoni. "HELIX: Automatic Parallelization of Irregular Programs for Chip Multiprocessing". Presented at the 10th International Symposium on Code Generation and Optimization (CGO). San Jose, California, USA. April 2nd, 2012.

9. Simone Campanoni. "HELIX: The Importance of Predictability". Presented at Princeton University - Princeton, USA. October 3, 2012. Invited talk.

10. Simone Campanoni. "Static Memory Management within Bytecode Languages on Multicore Systems". Presented at the Workshop on Computing in Heterogeneous, Autonomous 'N' Goal-oriented Environments (CHANGE). Newport Beach, California. March 6th, 2011.

11. Simone Campanoni. "ILDJIT: A compilation framework for CIL bytecode". Presented at Harvard University - Cambridge, USA. April 28, 2010. Invited talk.

12. Simone Campanoni. "ILDJIT: A compilation framework for CIL bytecode". Presented at Microsoft Research - Seattle, USA. March 22, 2010. Invited talk.

13. Simone Campanoni. "Dynamic Compilation and Parallelism: Theory and large scale experimentation". Presented at the PhD dissertation. Milan, Italy. March, 2009.

14. Simone Campanoni. "Parallelism on compilation and execution". PhDay at Politecnico di Milano. Milan, Italy. June 24th, 2009.

15. Simone Campanoni. "Traces of control-flow graphs". Presented at 13th International Conference on Developments in Language Theory (DLT). Stuttgart University, Germany. June 30, 2009.

16. Simone Campanoni. "Dynamic Look Ahead Compilation: a technique to hide JIT compilation latencies in multicore environment". Presented at 18th International Conference on Compiler Construction (CC). York, United Kingdom. March 24, 2009.

17. Simone Campanoni. “A parallel dynamic compiler for CIL bytecode”. Presented at PhDay at Politecnico di Milano. Milan, Italy. June 26th, 2008.

18. Simone Campanoni. “Traces of control-ow graphs: a feasibility study of using trace theory for compilation”. Presented at “Developments and New Tracks in Trace Theory” workshop, Cremona, Italy, October 11, 2008. Invited talk.

19. Simone Campanoni. “Node-Level Optimization of Wireless Sensor Networks”. Presented at IEEE 2008 Wireless Communications, Networking and Mobile Computing (WiCOM). Dalian, China. October 13, 2008.

20. Simone Campanoni. “Models and Tradeoffs in WSN System-Level Design”. Presented at IEEE 2008 International Conference on Digital System Design (DSD). Parma, Italy. September 4, 2008.

21. Simone Campanoni. “Multi-level Design and Optimization of Wireless Sensor Networks”. Presented at IEEE 2008 International Conference on Networked Sensing Systems (INSS). Kanazawa, Japan. June 18, 2008.

22. Simone Campanoni. “Ensuring Feasibility of Wireless Sensor Networks”. Presented at IEEE 2008 International Conference on Circuits and Systems for Communications (ICCSC). Shanghai, China. May 27, 2008.

23. Simone Campanoni. “ILDJIT: a parallel dynamic compiler”. Presented at 16th IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC). Rhodes Island, Greece. October 14, 2008.

24. Simone Campanoni. “SWORDFISH: a Framework to Formally Design WSNs Capturing Events”. Presented at IEEE 2007 International Conference on Software, Telecommunications and Computer Networks (SoftCOM). Split-Dubrovnik, Croatia. September 27, 2007.

25. Simone Campanoni. “Common Language Infrastructure (CLI)”. Presented at Linux Day - Varese, Italy. October 5, 2007. Invited talk.

26. Simone Campanoni. “Intermediate Language Distributed Just In Time for the CIL Bytecode”. Presented at the master thesis. Milan, Italy. July, 2006.

27. Simone Campanoni. “DotGNU”. Presented at Linux Day - Sesto Calende, Italy. October 8, 2006. Invited talk.

28. Simone Campanoni. “Ontology Packet Manager”. Presented at the bachelor thesis. July, 2004.

TEACHING EXPERIENCE

Course Instructor

Politecnico di Milano Computer Science Parallelism Course: Parallelism in wonderland: are you ready to see how deep the rabbit hole goes? String 2014. With Marco D. Santambrogio.

Harvard University Computer Science 253r: Virtual Machines. Fall 2010. With Vijay Janapa Reddi.

Teaching Assistance

November 2008 – January 2009 Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.

November 2008 – January 2009 Formal languages and compilers course at Politecnico di Milano university.

March 2008 – July 2008 Software engineering at Politecnico di Milano university.

November 2007 – January 2008 Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.

November 2007 – January 2008 Formal languages and compilers course at Politecnico di Milano university.

March 2007 – July 2007 Software engineering at Politecnico di Milano university.

November 2006 – January 2007 Trasformazione e ottimizzazione del codice (a compiler optimization course) at Politecnico di Milano university.

October 2006 – January 2007 Informatica B laboratory at Politecnico di Milano university.

Co-advisor in thesis

2015 *Niall Murphy*. Expected to get his Ph.D. degree in 2015. Advisor: Prof. Robert Mullins.

2015 *Kevin Brownell*. Expected to get his Ph.D. degree in June 2015. Advisor: Prof. David Brooks.

2012 *Pietro Malossi*. "Achieving Platform-Independence for the ILDJIT Compilation Framework". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2011 *Andrea Cazzaniga*. "Runtime threads managing in ILDJIT". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Marco Domenico Santambrogio.

2011 *Diego Mereghetti*. "Definizione di un supporto alla compilazione Just in Time nell'ambito dei sistemi auto adattativi". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Marco Domenico Santambrogio.

2010 *Luca Rocchini*. "Supporto alla programmazione generica nel compilatore ILDJIT". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Stefano Anelli*. "Method specialization for Common Intermediate Language in a dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Ettore Speziale*. "Multithreading support in ILDJIT dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Michele Tartara*. "ARM code generation and optimization in a dynamic compiler". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2009 *Marcello Boiardi*. "Scelta automatica di algoritmi di ottimizzazione di codice all'interno del compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Cremona, Italy. Advisor: Prof. Pierluigi San Pietro.

2009 *Massimiliano Grandi*. "Supporto delle caratteristiche di introspezione dello standard ECMA-335 nel compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Cremona, Italy. Advisor: Prof. Pierluigi San Pietro.

2008 *Massimiliano Manni, Roberto Molteni*. "Progetto ed implementazione di librerie interne per il supporto dello standard ECMA-335 nel compilatore dinamico ILDJIT". Bachelor of Science in Information Technology, BSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. Stefano Crespi Reghizzi.

2008 *Alessandro Assinnata*. "Pianificazione di WSN". Master of Science in Information Technology, MSc-IT, Politecnico di Milano, Milano, Italy. Advisor: Prof. William Fornaciari.

WORKING EXPERIENCE

November 2012 – Current Research Associate at Harvard University.

November 2009 – October 2012 Postdoctoral Position at Harvard University under both Prof. David Brooks and Prof. Gu-yeon Wei.

July 2001 – April 2002 Civil service at Gulliver in Cantello (Varese).

Febr. 2001 – July 2001 Industry worker at Suprema Oggiona S.Stefano building cash registers.

SOFTWARE AND TOOLS

2010 – Current Developed a GPL licensed parallelizing compiler called **HELIX**

Website http://helix.eecs.harvard.edu

2005 – 2014 Developed a GPL licensed compilation framework called **ILDJIT** for the Common Language Infrastructure (CLI) described in the ECMA-335 standard.

Website http://ildjit.sourceforge.net

2006 – 2008 Developed a GPL licensed framework to deploy automatically wireless sensors networks (Swordfish).

2006 Extended the tuple-based middleware "TinyLime" to exploit sensors. The software has been used in the article "Pervasive games in a mote-enabled virtual world using tuple space middleware". Luca Mottola, Amy Murphy and Gian Pietro Picco. NetGames'06.

2005 – 2006 Developed a GPL licensed framework for developing agents based on the WSS project.

2004 – 2005 Developed a GPL licensed world simulator (WSS) for a GNU/Linux system to support the planning of sensor networks using a logic language as input.

2004 Developed a GPL licensed ontology packet manager for the GNU/Linux systems.

INTERNATIONAL SCIENTIFIC COLLABORATION

Visiting experiences

January 2014 A week visit at University of Cambridge to collaborate with Dr. Timothy M. Jones and Prof. Robert Mullins in the context of the HELIX project.

August 2008 – November 2008 Three months visit at Harvard University. I have been involved in the ALARM research project, which is about the hardware process variation problem, under the supervision of Prof. Gu-Yeon Wei and Prof. David Brooks. I designed and implemented the code scheduler algorithm to dynamically reduce the fluctuation of the internal voltage of CPUs.

Participation in research projects

2007 – 2009 I have been involved in the OMP European research project at Politecnico di Milano. I was responsible to design and implement a dynamic compiler for the CIL bytecode language for ARM-based embedded platforms.

Past and current collaborators

- Princeton University
- University of Cambridge
- Harvard University
- Politecnico di Milano
- Freescale Semiconductor
- ST Microelectronics
- INRIA

EDUCATION

January 2007 — 2009 Ph.D. studies in Information Technologies at Politecnico di Milano. The Ph.D. was concluded with the highest honors. The advisor was Professor Stefano Crespi Reghizzi

Sept. 2004 — July 2006 Engineering studies at Politecnico di Milano, where he has been awarded the "Laurea specialistica" (Master of Science) degree in "Ingegneria Informatica" (Computer Engineering) with 110 Lode as final mark. Details on the programs can be found at http://www.dei.polimi.it

During the studies, developed a tuple based middle-ware extension for the TinyLime based on Lime and TinyOS that allows tuples to be sent on sensors.

In 2005-2006 he has worked on his thesis on an innovative project, building a new distributed virtual machine for the CLI architecture described in the ECMA 335 standard (DotNET). The thesis advisors were Prof. Stefano Crespi Reghizzi and Ing. Giovanni Agosta.

Sept. 2001 — July 2004 Engineering studies at Politecnico di Milano, where he has been awarded the "Laurea triennale" (Bachelor of Science) degree in "Ingegneria Informatica" (Computer Engineering) with 108 as final mark.

In 2004 he has worked on his thesis on an innovative project, building an ontology packet manager for the GNU/Linux systems. The thesis advisor was Prof. Marco Colombetti.

Sept. 1995 — July 2000 High-school education at ITIS of Gallarate "Roberto Franceschi" on Telecomunication and electronics.

School Participation

Summer 2007 ACACES: Summer School on Advanced Computer Architecture and Compilation for Embedded Systems

COMPUTER SKILLS

Simone has learned to use the following programming languages and systems:

- Compiler internals: ILDJIT, LLVM, GCC.
- Compiler construction tools: Lex, Bison (Yacc), LLVM, Libjit.
- Programming tools: automake, autoconf, aclocal, libtool, pkg-config, gcc, gdb, PIN, gprof, gperf, valgrind, Intel VTune, Intel PTU.
- Versioning systems: git, bazaar, subversion, cvs.
- Operating Systems: GNU/Linux, GNU/Hurd, TinyOS (including kernel development and network administration).
- Programming languages: C, C++, C#, Java, Lisp, bash scripting, PHP, Perl, Python, NesC.
- Markup languages: XML.
- Programming frameworks: Allegro, Apache.
- Middleware: Lime, TinyLime, Corba, ONC RPC, Java RMI.
- Database management systems: PostgreSQL, mySQL.
- Document writing: Latex.

MISCELLANEOUS

- HiPEAC member
- IEEE member

REFERENCES

- Prof. David Brooks
  Gordon McKay Professor of Computer Science
  Harvard University
  Maxwell Dworkin 141
  33 Oxford Street, Cambridge MA 02138

- Prof. Gu-Yeon Wei
  Professor of Electrical Engineering
  Harvard University
  Maxwell Dworkin 343
  33 Oxford Street, Cambridge MA 02138

- Prof. David I. August
  Professor of Computer Science
  Princeton University
  Computer Science Building Room 221
  35 Olden Street, Princeton NJ 08544

- Prof. Stefano Crespi Reghizzi
  Professor of Electrical Engineering
  Politecnico di Milano
  DEIB Building
  Ponzio 34, Milan 20133 Italy

- Prof. Timothy Sherwood
  Professor of Computer Science
  University of California Santa Barbara
  Department of Computer Science Office 1119
  Harold Frank Hall, Santa Barbara, CA 93106-5110

- Prof. Albert Cohen
  Associate Professor of Computer Science
  Ecole Polytechnique
  Rataud building office S11
  rue d'Ulm 45, Paris 75005 France
  Senior Research Scientist at INRIA