

Xiaoyao Liang

Curriculum Vitae

Harvard University
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RESEARCH INTERESTS

Variation tolerant circuits and microarchitecture, reconfigurable and power-aware embedded systems, VLSI circuits, architectures and EDA tools for the nano-scale technologies, multi-core and multi-processor architectures for biology and scientific applications

EDUCATION

Harvard University	12/2008
Ph. D Computer Architecture, VLSI	
State University of New York at Stony Brook	12/2004
Master VLSI	
Fudan University	07/2000
Bachelor Telecommunication	

PROFESSIONAL EXPERIENCE

Intel Oregon Microarchitecture Lab, Research Intern	07/2008-10/2008
● <u>Comprehensive Fault-Tolerant Microarchitecture Design</u> Conducted research on comprehensive fault-tolerant microarchitecture design. Proposed novel and flexible error correction scheme which can adapt to the error heuristics and aging of the devices.	
IBM T.J Watson Research Center, Research Intern	06/2007-09/2007
● <u>EDA Tool for Automatic FPGA Partitioning</u> Designed EDA tool for automatic FPGA partitioning. Tool can automatically partition large digital design into multiple FPGAs, insert SEDERS at FPGA boundaries, guarantee correct timing for transmitter and receiver.	
LDIC Electronics Tech Inc., ASIC Engineer	01/2003-07/2003
● <u>Design of 100M/1000M Ethernet Switch</u> Designed layer two ethernet switch MAC controller, including receive and transmit module, FIFO managing and address learning module. Chip was successfully taped out and silicon verified.	
Divio Inc., ASIC Engineer	12/2001-12/2002
● <u>Design of ARM Core Based System on Chip (SoC)</u>	

Participated in the whole chip architecture and specification design. RTL design of AMBA supported system components. Established chip level verification.

- *Design of USB Digital Image Camera*
Designed USB Function Controller compatible with USB Rev 1.1 specification. Synthesis, STA, formality test and DFT was performed. Chip was successfully taped out and silicon verified.

Ali Corporation, ASIC Engineer 07/2000-11/2001

- *Design of Baseband OFDM Chip for Wireless LAN (IEEE 802.11a)*
Adopted carrier frequency acquisition loop and lock frequency method for symbol timing recovery. Study in complexity and accuracy trade-off.
- *Design of Baseband Transceiver Chip for Wireless LAN (IEEE 802.11b)*
Developed a maximum-likelihood based estimation scheme for channel estimation, with applications in design of low-complexity and fast converging equalizer. This chip was successfully taped out and silicon verified.

RESEARCH EXPERIENCE

Harvard University, Research Assistant 02/2005-12/2008

Working in the Computer Architecture and VLSI lab. Research focuses on exploring novel architectures, CAD, and circuit solutions that are aware of upcoming design challenges such as process, temperature and voltage variations. Research also includes performance and power modeling for modern processors.

- *Testing and Design Strategies for Microarchitecture Post-Fabrication Tuning*
This testing and design framework uses on-chip canary circuits to capture systematic variation while using statistical analysis to estimate random variation. Regression model is applied to predict the chip performance and power. These techniques comprise an integrated framework that identifies the most energy efficient post-fabrication tuning configuration for each chip.
- *ReViVaL: Variable Pipeline Latency and Voltage Interpolation for Process Variations*
Developed two novel technologies that can be used for fine-grain, post-fabrication chip tuning, to reduce the frequency penalty due to process variation. Prototype chips were fabricated for validation of the proposed technology. Combined with architecture study shows significant advantages over traditional designs.
- *Next Generation Variation Tolerant On-Chip Memory Design*
Proposed to replace 6T-based SRAM with 3T1D-based DRAM for processor data caches. This eliminates the memory stability issues under variation. Combined with smart refresh policies, the proposed schemes achieve much better variation tolerance. One paper related to this project was selected into “Micro top picks”, which collects 10 most industry relevant and outstanding architecture papers in 2007.
- *Microarchitecture Parameter Selection Under the Impact of Process Variations*
Proposed a method of selecting microarchitectural parameters to mitigate the frequency impact due to process variability for distinct structures, while minimizing IPC loss. We proposed an optimization procedure to be used for system-level design decisions, and we find that joint architecture and statistical timing analysis can be more advantageous than pure circuit level optimization.

- Highly Accurate SRAM and CAM Power Modeling for Early Stage Architecture Design

Developed hybrid empirical and analytical power modeling method for memory structures based on small block Hspice simulations. This method can be easily integrated into existing cycle-accurate simulators for power analysis. Compared with traditional tools, this scheme achieves better accuracy or less simulation overhead.

State University of New York at Stony Brook, Research Assistant 09/2003-12/2004
Working in VLSI system design lab. Research focuses on innovative VLSI architectures, algorithms and design for signal processing systems and highly reconfigurable systems.

- Buffer-Level pipelining Data Centric Design Methodology
Applied buffer-level pipelining data centric design methodology to dynamically reconfigure the embedded system for the application of different types of particle filters. FPGA prototyping verified this method can maximally utilize the hardware resource with minimum reconfiguration overhead.

TEACHING EXPERIENCE

Harvard University, Teaching Fellow 02/2007-5/2008
Served as a teaching fellow for Computer Architecture (CS141), VLSI Circuits and Systems (CS148) and Mixed-Signal IC Design (ES271r).

Co-Supervised Undergraduate and MS Students

- Kristen Elizabeth Lovin
Topic: Variation and power modeling for 3T1D memory
- Ali Durlav Khan
Topic: Testing of the prototype floating-point unit with ReVIVaL
- Hien Do
Topic: Power and performance modeling of the peripheral SRAM circuits
- Kerem Turgay
Topic: Power and performance modeling of CAM based memory
- John Lai
Topic: Power and performance modeling of CAM based memory

State University of New York at Stony Brook, Teaching Assistant 09/2003-12/2004
Served as a teaching assistant for Computer Architecture (ESE345), VLSI System Design (ESE555).

HONORS AND AWARDS

- Papers selected into IEEE Micro's "Top Picks in Computer Architecture" special issues. "Top Picks" is awarded to 10 most outstanding and industry relevant architecture papers annually. 2007, 2008
- Won first prize of SRC SoC IC Design Challenge. This was awarded to the champion of 55 teams from top American universities. 2005-2006
- Harvard DEAS Fellowship 2005-2006
- Stony Brook President Scholarship 2003-2004
- Fudan Scholarship of Excellence 1996-2000
- Siemens International Student Circle. This was awarded to students with balanced

PRESS RELEASE

- “Semiconductor Industry Initiatives Seek to Capture EE Student Interest, Increase Retention” --- IEEE-USA Today’s Engineer
- “Student teams win \$15,000 for SoC designs” --- EETimes
- “SRC/SIA SoC Design Challenge” --- SRC
- “SRC, SIA Tackle Ultra-Low Power SoC Design Challenges for ‘Extremely Scaled’ Silicon via University Competition Results” --- Business Wire

JOURNAL PUBLICATIONS

- **Xiaoyao Liang**, Gu-Yeon Wei and David Brooks, “ReVIVaL, Variation Tolerant Architecture Using Voltage Interpolation and Variable Latency,” *IEEE Micro Top Picks*, January 2009.
- **Xiaoyao Liang**, Ramon Canal, Gu-Yeon Wei and David Brooks, “Replacing 6T SRAMs with 3T1D DRAMs in the L1 Data Cache to Combat Process Variability,” *IEEE Micro Top Picks*, January 2008.

CONFERENCE PUBLICATIONS

- Gu-Yeon Wei, David Brooks, A. Durlow Khan, **Xiaoyao Liang**, “Instruction-Driven Clock Scheduling with Glitch Mitigation,” *International Symposium on Low Power Electronics and Design (ISLPED 2008)*, August 2008.
- **Xiaoyao Liang**, Gu-Yeon Wei, David Brooks, “ReVIVaL: A Variation Tolerant Architecture Using Voltage Interpolation and Variable Latency,” *International Symposium on Computer Architecture (ISCA-35)*, June 2008.
- **Xiaoyao Liang**, Gu-Yeon Wei, David Brooks, “A Process-Variation-Tolerant Floating-Point Unit with Voltage Interpolation and Variable Latency,” *IEEE International Solid State Circuit Conference (ISSCC 2008)*, February 2008.
- **Xiaoyao Liang**, Ramon Canal, Gu-Yeon Wei, David Brooks, “Process Variation Tolerant 3T1D-based Cache Architectures,” *40th International Symposium on Microarchitecture (MICRO-40)*, December 2007.
- **Xiaoyao Liang**, Kerem Turgay, David Brooks, “Architectural Power Models for SRAM and CAM Structures Based on Hybrid Analytical/Empirical Techniques,” *International Conference on Computer Aided Design (ICCAD-07)*, November 2007.
- **Xiaoyao Liang** and David Brooks, “Mitigating the Impact of Process Variations on CPU Register File and Execution Units,” *39th International Symposium on Microarchitecture (MICRO-39)*, December 2006.
- **Xiaoyao Liang** and David Brooks, “Microarchitecture Parameter Selection to Optimize System Performance under Process Variation,” *International Conference on Computer Aided Design (ICCAD-06)*, November 2006.
- **Xiaoyao Liang** and David Brooks, “Highly Accurate Power Modeling Method for SRAM Structures with Simple Circuit Simulation,” *The Second Watson Conference on Interaction between Architecture, Circuits, and Compilers (p=ac2)*, September, 2005.
- **Xiaoyao Liang**, A. Athalye, Sangjing Hong, “Equalizing Execution Path for

Processing Speed Determination in Block Level Pipelining,” *IEEE International Symposium on Circuits and Systems (ISCAS-05)*, May 2005.

- **Xiaoyao Liang**, A. Athalye, Sangjing Hong, “Dynamic Coarse Grain Dataflow Reconfiguration Technique for Real-Time System Design,” *IEEE International Symposium on Circuits and Systems (ISCAS-05)*, May 2005.
- Mark Hempstead, **Xiaoyao Liang**, Patrick Mauro, Gu-Yeon Wei, David Brooks, “Design and Implementation of An Ultra Low Power System Architecture for Wireless Sensor Network Applications,” *SRC Techcon, SoC Design Contest*, October 2005.
- Yulei Weng, Sankalp Kallakuri, **Xiaoyao Liang**, Alex Doholi, et. al, “Dynamic Architecture Adaptation to Improve Scalability of Sensor Networks: A Case Study for a Smart Sensor for Face Recognition,” *25th IEEE International Real-Time Systems Symposium (RTSS-04)*, December, 2004.
- Sangjin Hong, **Xiaoyao Liang**, M. Bolic, P. M. Djuric, “Data Centric SIR Particle Filter Design Using Buffer-level Pipelining”, *7th International Conference on Signal Processing (ICSP-04)*, August 2004.
- Sangjin Hong, **Xiaoyao Liang**, M. Bolic, P. M. Djuric, “Design and Synchronization of Gaussian Particle Filter Using Distributed Controller Scheme”, *7th International Conference on Signal Processing (ICSP-04)*, August 2004.
- Sangjin Hong, M. Sadasivam, **Xiaoyao Liang**, “Post-Generation of Overall Execution Controller for Data Centric Signal Processing Algorithms,” *7th International Conference on Signal Processing (ICSP-04)*, August 2004.

WORKSHOP PUBLICATIONS

- **Xiaoyao Liang**, Ramon Canal, Gu-Yeon Wei, David Brooks, “Process Variation Tolerant Register Files Based on Dynamic Memories,” *Workshop on Architectural Support for Gigascale Integration (ASGI'07)*, in conjunction with ISCA 2007, June 2007.
- **Xiaoyao Liang** and David Brooks, “Latency Adaptation for Multi-ported Register Files to Mitigate the Impact of Process Variations,” *Workshop on Architectural Support for Gigascale Integration (ASGI'06)*, in conjunction with ISCA 2006, June 2006.
- Sangjin Hong, **Xiaoyao Liang**, P. M. Djuric, “Reconfigurable Particle Filter Design Using Dataflow Structure Translation”, *IEEE Workshop on Signal Processing Systems (SIPS'04)*, September 2004.

PATENTS

- **Xiaoyao Liang**, David Brooks, Gu-Yeon Wei, “Process Variation Tolerant Circuit with Voltage Interpolation and Variable Latency”, *US Patent Application #: 12,261,771*, October, 2008.

TALKS

- “ReVIVaL: Variation Tolerant Architecture” 06/2008
International Symposium on Computer Architecture Beijing, China
- “Variation Tolerant FPU Design with ReVIVaL” 02/2008

- International Solid State Circuit Conference San Francisco, USA
“3T1D-Based Cache Architecture” 12/2007
- International Symposium on Microarchitecture Chicago, USA
“Hybrid Power Models for CAM and SRAM” 11/2007
- International Conference on Computer Aided Design San Jose, USA
“FPGA Partitioning with SERDES Insertion” 08/2007
- IBM T.J Watson Research Center Yorktown Heights, USA
“3T1D-Based Register Files” 06/2007
- ASGI with ISCA San Diego, USA
“Mitigating Variations in Processor RF and Execution Units” 12/2006
- International Symposium on Microarchitecture Orlando, USA
“Processor Parameter Selection with Variations” 11/2006
- International Conference on Computer Aided Design San Jose, USA
“Latency Adaptation for Register Files” 06/2006
- ASGI with ISCA Boston, USA
“Hybrid Power Modeling for SRAM” 09/2005
- IBM T.J Watson Research Center Yorktown Heights, USA

PAPER REVIEWS

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- International Symposium on Low Power Electronics and Design 2006-2008
 - International Symposium on Computer Architecture 2008
 - IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2008
 - International Symposium on Microarchitecture 2007
 - High Performance Computer Architecture 2007
 - International Conference on Computer Design 2006-2007
 - Architectural Support for Programming Languages and Operating Systems 2006
 - International Symposium Performance Analysis of Systems and Software 2006

REFERENCE

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