

Xiaoyao Liang

Resume

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CAREER HIGHLIGHTS

- Four chips designed were successfully taped out and silicon verified
- More than ten first author papers published at premier conferences
- One paper was selected into 2007 Micro Top Picks
- First prize winner of SRC SoC design contest 2005-2006
- More than seven years of solid VLSI and ASIC design experience
- Ample research and working experience in world famous universities and companies

EDUCATION

Harvard University 12/2008 (expected)
Ph. D Computer Architecture, VLSI

State University of New York at Stony Brook 12/2004
Master VLSI

Fudan University 07/2000
Bachelor Telecommunication

PROFESSIONAL EXPERIENCE

Intel Oregon Microarchitecture Lab, Research Intern 07/2008-10/2008

- Comprehensive Fault-Tolerant Microarchitecture Design
Conducted research on comprehensive fault-tolerant microarchitecture design. Proposed novel and flexible error correction scheme which can adapt to the error heuristics and aging of the devices.

IBM T.J Watson Research Center, Research Intern 06/2007-09/2007

- EDA Tool for Automatic FPGA Partitioning
Designed EDA tool for automatic FPGA partitioning. Tool can automatically partition large digital design into multiple FPGAs, insert SEDERS at FPGA boundaries, guarantee correct timing for transmitter and receiver.

LDIC Electronics Tech Inc., ASIC Engineer 01/2003-07/2003

- Design of 100M/1000M Ethernet Switch
Designed layer two ethernet switch MAC controller, including receive and transmit module, FIFO managing and address learning module. Chip was successfully taped out and silicon verified.

Divio Inc., ASIC Engineer

12/2001-12/2002

- Design of ARM Core Based System on Chip (SoC)
Participated in the whole chip architecture and specification design. RTL design of AMBA supported system components. Established chip level verification.
- Design of USB Digital Image Camera
Designed USB Function Controller compatible with USB Rev 1.1 specification. Synthesis, STA, formality test and DFT was performed. Chip was successfully taped out and silicon verified.

Ali Corporation, ASIC Engineer

07/2000-11/2001

- Design of Baseband OFDM Chip for Wireless LAN (IEEE 802.11a)
Adopted carrier frequency acquisition loop and lock frequency method for symbol timing recovery. Study in complexity and accuracy trade-off.
- Design of Baseband Transceiver Chip for Wireless LAN (IEEE 802.11b)
Developed a maximum-likelihood based estimation scheme for channel estimation, with applications in design of low-complexity and fast converging equalizer. This chip was successfully taped out and silicon verified.

RESEARCH EXPERIENCE**Harvard University, Research Assistant**

02/2005-Present

Working in the Computer Architecture and VLSI lab. Research focuses on exploring novel architectures, CAD, and circuit solutions that are aware of upcoming design challenges such as process, temperature and voltage variations. Research also includes performance and power modeling for modern processors.

- ReViVaL: Variable Pipeline Latency and Voltage Interpolation for Process Variations
Developed two novel technologies that can be used for fine-grain, post-fabrication chip tuning, to reduce the frequency penalty due to process variation. Prototype chips were fabricated for validation of the proposed technology. Combined with architecture study shows significant advantages over traditional designs.
- Next Generation Variation Tolerant On-Chip Memory Design
Proposed to replace 6T-based SRAM with 3T1D-based DRAM for processor data caches. This eliminates the memory stability issues under variation. Combined with smart refresh policies, the proposed schemes achieve much better variation tolerance. One paper related to this project was selected into “Micro top picks”, which collects 10 most industry relevant and outstanding architecture papers in 2007.
- Microarchitecture Parameter Selection Under the Impact of Process Variations
Proposed a method of selecting microarchitectural parameters to mitigate the frequency impact due to process variability for distinct structures, while minimizing IPC loss. We proposed an optimization procedure to be used for system-level design decisions, and we find that joint architecture and statistical timing analysis can be more advantageous than pure circuit level optimization.
- Highly Accurate SRAM and CAM Power Modeling for Early Stage Architecture Design
Developed hybrid empirical and analytical power modeling method for memory structures based on small block Hspice simulations. This method can be easily

integrated into existing cycle-accurate simulators for power analysis. Compared with traditional tools, this scheme achieves better accuracy or less simulation overhead.

State University of New York at Stony Brook, Research Assistant 09/2003-12/2004
Working in VLSI system design lab. Research focuses on innovative VLSI architectures, algorithms and design for signal processing systems and highly reconfigurable systems.

- *Buffer-Level pipelining Data Centric Design Methodology*
Applied buffer-level pipelining data centric design methodology to dynamically reconfigure the embedded system for the application of different types of particle filters. FPGA prototyping verified this method can maximally utilize the hardware resource with minimum reconfiguration overhead.

HONORS AND AWARDS

- One paper selected into Micro Top Picks 2007
Awarded to 10 most outstanding and industry relevant architecture papers of the year
- First prize winner, final of SRC SoC Design Challenge 2005-2006
Awarded to the champion of 55 teams from top American universities
- Harvard DEAS Fellowship 2005-2006
Awarded to excellent Ph. D candidates
- Stony Brook President Scholarship 2003-2004
Awarded to excellent Ph. D candidates
- Fudan Scholarship of Excellence 1996-2000
Awarded to top 15% undergraduate students
- Siemens International Student Circle 1999
Awarded to students with balanced academic and extra-curriculum achievements

SELECTED PUBLICATIONS

- **Xiaoyao Liang**, Ramon Canal, Gu-Yeon Wei and David Brooks, "Replacing 6T SRAMs with 3T1D DRAMs in the L1 Data Cache to Combat Process Variability," *Micro Top Picks*, January 2008.
- **Xiaoyao Liang**, Gu-Yeon Wei and David Brooks, "ReVIVaL: A Variation Tolerant Architecture Using Voltage Interpolation and Variable Latency," *International Symposium on Computer Architecture (ISCA-35)*, June 2008.
- **Xiaoyao Liang**, Gu-Yeon Wei and David Brooks, "A Process-Variation-Tolerant Floating-Point Unit with Voltage Interpolation and Variable Latency," *IEEE International Solid State Circuit Conference (ISSCC 2008)*, February 2008.
- **Xiaoyao Liang**, Ramon Canal, Gu-Yeon Wei and David Brooks, "Process Variation Tolerant 3T1D-based Cache Architectures," *40th International Symposium on Microarchitecture (MICRO-40)*, December 2007.
- **Xiaoyao Liang**, Kerem Turgay and David Brooks, "Architectural Power Models for SRAM and CAM Structures Based on Hybrid Analytical/Empirical Techniques," *International Conference on Computer Aided Design (ICCAD-07)*, November 2007.
- **Xiaoyao Liang** and David Brooks, "Mitigating the Impact of Process Variations on CPU Register File and Execution Units," *39th International Symposium on Microarchitecture (MICRO-39)*, December 2006.
- **Xiaoyao Liang** and David Brooks, "Microarchitecture Parameter Selection to

Optimize System Performance under Process Variation,” *International Conference on Computer Aided Design (ICCAD-06)*, November 2006.

- **Xiaoyao Liang**, A. Athalye and Sangjing Hong, “Equalizing Execution Path for Processing Speed Determination in Block Level Pipelining,” *IEEE International Symposium on Circuits and Systems (ISCAS-05)*, May 2005.
- **Xiaoyao Liang**, A. Athalye and Sangjing Hong, “Dynamic Coarse Grain Dataflow Reconfiguration Technique for Real-Time System Design,” *IEEE International Symposium on Circuits and Systems (ISCAS-05)*, May 2005.

SKILLS

- **Logic Modeling and Verification:** Verilog, NC-Verilog, VCS, Formality
- **FPGA Prototyping:** Xilinx ISE, Altera Quartus, Synplicity
- **Synthesis and Timing:** Synopsys Design Compiler, Prime Time, Cadence Ambit
- **Circuit Simulation:** Hspice, Spectre, Nanosim
- **Schematic and Layout:** Cadence Virtuoso, Silicon Ensemble, Synopsys Astro
- **Software:** MATLAB, C
- **System Modeling:** SystemC, Co-centric
- **Others:** C_shell, Tcl_shell, Perl, Latex

REFERENCE

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