Course Outline

- Instructor
- Prerequisites
- Topics of Study
- Course Expectations
- Grading
- Class Scheduling Conflicts
Instructor

- Instructor: David Brooks (dbrooks@eecs.harvard.edu)
  - Office Hours: TBD, MD141, stop by/email whenever
Prerequisites

- **CS141** (or equivalent)
  - Digital Logic/Pipelined Processors
  - i.e. Hennessey & Patterson Jr. (HW/SW Interface)
- **CS146** is good, but not necessary
  - Hennessey & Patterson Sr. (Quantitative) Computer Architecture
- If not much architecture background, but interested in low-power design
  - Background in one of compilers, OS, or Circuits/VLSI should be good enough
  - You will become the discussion leader in the power-aware OS/compiler/Ckts papers
- **C Programming**, **UNIX for Project** (or similar skills)
Topics of CS246

• Introduction to Power-Aware Computing
• Architectural Level Power Modeling
• OS Level Power Modeling/Measurement
• Chip and System Level Temperature Modeling
• Newer Trends in Power-Aware Computing (di/dt, reliability, leakage power, etc)
• Architectural, Compiler, and O/S Techniques to reduce power/temperature/etc
  – Chip/HW level techniques
  – OS/Compiler/Software techniques
  – Data center energy management
Detailed Topics from Last Year

• High-level Power modeling (power abstractions)
• Power Measurement for OS control
• Temperature Aware Computing
• Di/Dt Modeling
• Leakage Power Modeling and Control
• Frequency and Voltage Scheduling Algorithms
• Power in Data Centers
• Dynamic Power Reduction in Memory
• Disk Power Modeling/Management
• Application and Compiler Power Management
• Dynamic adaptation for Multimedia applications
• Intel XScale Microprocessor, IBM Watchpad
• Human Powered Computing
Course Expectations

• Seminar style course:
  – Expectation: you will read the assigned papers before class so we can have a lively discussion about them
  – Will setup online-web page to post comments/questions/discussion before class
  – Paper reviews – very short “paper review” highlighting interesting points, strengths/weaknesses of the paper
  – Discussion leadership – somewhere in the middle of the semester students will be assigned to present the paper/lead the discussions
Course Expectations

• Course project
  – Several possible ideas will be given
  – Also you may come up with your own
  – Depending on enrollment, I will schedule weekly/bi-weekly meetings with each individual/group (1/2hr per project) to discuss results/progress
  – There will be two presentations
    • First, a short “progress update” (before Winter break)
    • Second, a final presentation scheduled at the end of reading week
    • Finally, a project writeup written in research paper style
Grading

• Grade Formula
  – Class Participation – 50%
  – Project (including final project presentation) – 50%
Class Scheduling

- Have some students who’d like to take the class, but conflict.
  - Any time besides MW 1-2:30 or T/Th 10-11:30
  - Maybe MW 11-12:30?
Why worry about power dissipation?

Battery life

Thermal issues: affect cooling, packaging, reliability, timing

Environment
Moore’s Law & Power Dissipation...
Power-Aware Needed across all computing platforms

- Mobile/portable (cell phones, laptops, PDA)
  - Battery life is critical
- Desktops/Set-Top (PCs and game machines)
  - Packaging cost is critical
- Servers (Mainframes and compute-farms)
  - Packaging limits
  - Volumetric (performance density)
Battery Capacity Projections

Expected battery lifetime increase over the next 5 years: 30 to 40%

From Rabaey, 1995
Where does the juice go in laptops?

- Others have measured ~55% processor increase under max load in laptops [Hsu+Kremer, 2002]
Packaging cost

From Cray (local power generator and refrigeration)...

Source: Gordon Bell, “A Seymour Cray perspective”
http://www.research.microsoft.com/users/gbell/craytalk/
Packaging cost

To today…

• IBM S/390: refrigeration:
  – Provides performance (2% perf for 10°C) and reliability

Source: R. R. Schmidt, B. D. Notohardjono “High-end server low temperature cooling”
IBM Journal of R&D
Intel Itanium packaging

Complex and expensive (note heatpipe)

Source: H. Xie et al. “Packaging the Itanium Microprocessor”
Electronic Components and Technology Conference 2002
P4 packaging

• Simpler, but still…

From Tiwari, et al., DAC98

Source: Intel web site
What happens when the CPU cooler is removed?

www.tomshardware.de
www.tomshardware.com
Cooking Aware Computing
Server Farms

• Internet data centers are like heavy-duty factories
  – e.g. small Datacenter 25,000 sq.feet, 8000 servers, 2MegaWatts
  – Intergate Datacenter, Tukwila, WA: 1.5 Mill. Sq.Ft, ~500 MW
  – Wants lowest net cost per server per sq foot of data center space

• Cost driven by:
  – Racking height
  – Cooling air flow
  – Power delivery
  – Maintenance ease (access, weight)
  – 25% of total cost due to power
Environment

• Environment Protection Agency (EPA): computers consume 10% of commercial electricity consumption
  – This incl. peripherals, possibly also manufacturing
  – A DOE report suggested this percentage is much lower (3.0-3.5%)
  – No consensus, but it’s still a lot
  – Interesting to look at the numbers:
    • http://enduse.lbl.gov/projects/infotech.html

• Data center growth was cited as a contribution to the 2000/2001 California Energy Crisis

• Equivalent power (with only 30% efficiency) for AC

• CFCs used for refrigeration

• Lap burn

• Fan noise
Now we know why power is important

• What can we do about it?

• Two components to the problem:
  – #1: Understand where and why power is dissipated
  – #2: Think about ways to reduce it at all levels of computing hierarchy
  – In the past, #1 is difficult to accomplish except at the circuit level
  – Consequently most low-power efforts were all circuit related
Modeling + Design

• First Component (Modeling/Measurement):
  – Come up with a way to:
    • Diagnose where power is going in your system
    • Quantify potential savings

• Second Component (Design)
  – Try out lots of ideas

• This class will focus on both of these at many levels of the computing hierarchy
Next Time

• Bit more overview, feel out background of class
• Course website:
  http://www.eecs.harvard.edu/~dbrooks/CS246.htm
• Paper readings for this week:
  – “Power-Aware Microarchitecture: Design and Modeling
    Challenges for Next-Generation Microprocessors,” IEEE MICRO.
  – “Power: A First-Class Architectural Design Constraint,” IEEE
    Computer
• Web Page Browsing:
  – Information Technology and Resource Use:
    http://enduse.lbl.gov/projects/infotech.html
• Questions?