An interline CCD imaging array with on-chip A/D conversion

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Abstract

In this paper we describe an interline CCD imaging array which features high-speed, on-chip, parallel A/D conversion. In addition, we present test results from fabricated devices. The imaging chip was fabricated through MOSIS in a double-poly $2.0\mu m$ CCD/CMOS technology on a chip with total area $2.25mm \times 2.22mm$. The chip is composed of two components, namely, a 28×39 pixel, interline imaging array and a bank of 39, single-slope CCD/CMOS A/D converters; the converters function in parallel to achieve effective high-speed A/D conversion. Chip output is a stream of 8-bit digital data in which each 8-bit value corresponds to the light level at a pixel. Once an image has been captured, a set of parallel CCD shift registers transfer the data one column at a time to the parallel A/D converters. The analog data from each column is then converted in parallel and the resulting digital values are read out serially. In each row, the area cost of the A/D conversion circuitry is approximately the area occupied by eight pixels. This cost scales with the number of rows and the number of bits desired for the digital output and not with the number of columns. Ultimately, counter and control circuitry used to drive the single slope conversion can all be implemented on-chip, resulting in a single chip imager with direct digital output.

1 Introduction

Raw, analog image data from CCD cameras is easier to analyze and process if it is first converted into a digital format. The standard technique for performing this A/D conversion is to connect a single, stand-alone, high-speed A/D converter to the analog output of the CCD imaging array. This approach could conceivably be applied in designing a single chip CCD imaging array with a digital output, but suffers from a number of drawbacks: the required A/D converter demands significant chip area, must be extremely high speed to able to convert the analog level of every pixel in the array at frame rates, is prone to noise coupling, and may require post-processing (like laser trimming) in order to work properly. Furthermore, only minimal gains result from combining two chips on a single substrate if only one connection between them is necessary.

We present here an alternative approach to performing an on-chip A/D conversion of interline CCD image array data, an approach which takes advantage of the inherent parallelism in CCD imaging arrays. Specifically, we get digital output from our imager directly by using a bank of simple, single-slope A/D converters, one converter per row, instead of by using a single, complex, off-chip A/D converter. Using this architecture, the analog to digital conversion of the image data is performed on an entire column of image data at once, after which the digital results of these conversions are sequentially output. Because multiple A/D converters are used [1], each converter can be far slower, hence far simpler, than would be a single A/D converter used to process the entire array. The chip described below points toward a fully integrated, single-chip electronic camera with digital output.

In the balance of this paper, we will completely describe the CCD interline imager with on-chip A/D conversion. Specifically, we will present the overall architecture, design, and theory of operation of the chip. In addition, we will describe the test apparatus as well as test results from prototype devices fabricated through MOSIS. The prototype we describe here demonstrates the functionality and feasibility of the imager. We will conclude our discussion by describing enhancements which will make future imagers with on-chip A/D conversion suitable for real applications.

2 CCD Imager Design and Implementation

The imaging chip presented in this paper is composed of two major sections, namely, an interline CCD imaging array and a single slope A/D converter. The interline imager is an array of photodiodes coupled with a set of CCD shift registers [2, 3]. Each shift register is responsible for transferring image charge from a single row of photodiodes. The single slope A/D converters are made up of three major pieces: a comparator bank for image charge processing; a set of CCD latches and shift registers which store and transfer the converted digital value; and a CCD digital output buffer.

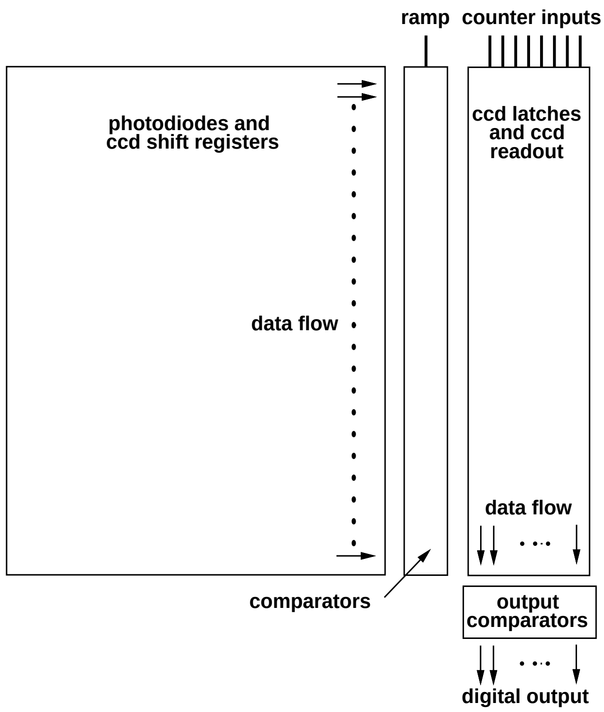

Figure 1: Block diagram of the interline imager chip with on-chip A/D conversion.

The overall imager is shown in block diagram form in figure 1 and in layout form in figure 2. The imager is implemented in $2\mu m$ double-poly, double metal, n-well CCD/CMOS technology on a chip with total area

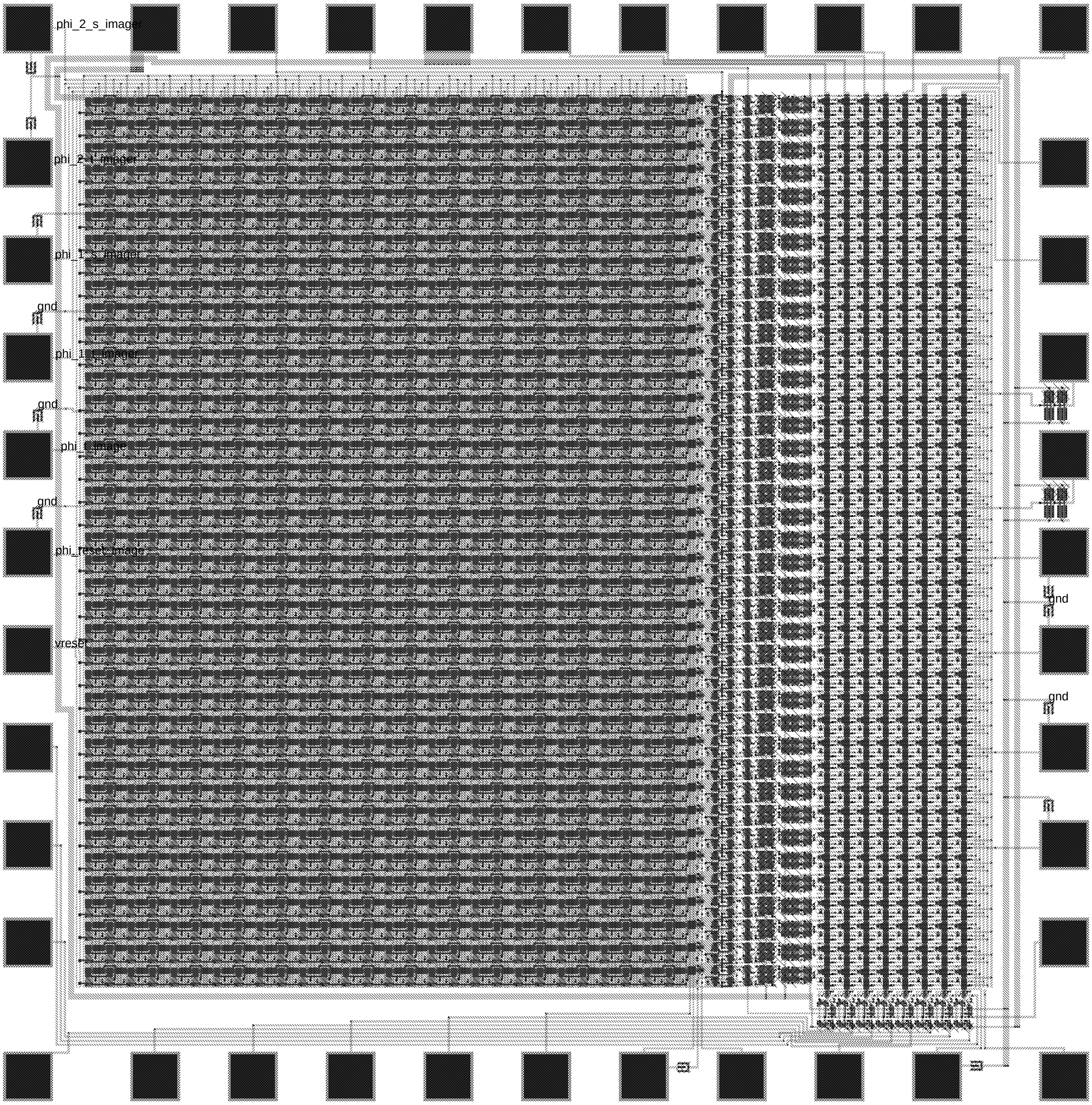

Figure 2: Layout of the interline imager chip with on-chip A/D conversion.

$2250\mu m \times 2220\mu m$ and photosensors distributed in a rectangular 28×39 array. The area of each pixel is $44\mu m \times 47\mu m$; each photojunction is approximately 5% of the total pixel area. The chips were fabricated through MOSIS at Orbit Semiconductor. For simplicity, all of the image transfer and digital output CCDs were implemented as surface channel devices. The output of the imager is an 8-bit digital data stream generated by the A/D converter bank. Each 8-bit output corresponds to a digital representation of the output of a single pixel. Image data is read out using a raster scan technique.

3 Imaging Array Operation

The imaging array with on-chip A/D conversion is designed to acquire an image and produce a data stream of 6- to 8-bit digital values corresponding to the image charge collected at each pixel. The first step in this process is the acquisition of image charge. The charge is next transferred into the image CCD shift registers and columnwise shifted to the A/D converter inputs. The A/D conversion is then performed on the image data, with the digital result, held by a set of CCD latches, represented by the presence or absence of charge in each latch. The final step in the array operation is the transfer of the 'digital' charge to output buffers which convert the digital charge packets to digital voltage outputs. Below, the operation of each subsystem in the chip will be described in greater detail.

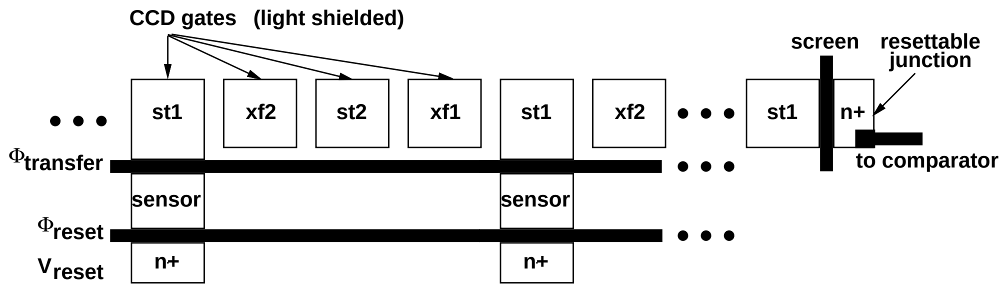

Figure 3: Schematic of the imaging and image data transfer subsystem.

The imaging and image data transfer portions of the chip, shown schematically in figure 3, function as follows. All of the photosensitive junctions are first strongly reverse biased using a whole-imager reset signal. The junctions are then allowed to float for a fixed amount of time, during which each pixel gathers photogenerated charge. A whole-imager transfer pulse is then used to shift this charge into the set of parallel image charge CCD shift registers; there is one image charge shift register per row. Each of these registers has its own pn junction output node. Image charge is transferred to this set of output nodes one column at a time.

Each output node and hence each imaging CCD row has a unique associated comparator; each output node is connected to the negative input of that comparator. The interface between the comparator, the imaging array, and the CCD latches is shown in figure 4. Once a column of image charge is transferred to the negative input of each comparators, the A/D conversion process begins. As the first step in the conversion, a high-to-low voltage ramp is fed to the positive input of the comparator in each row. This ramp is synchronized with an off-chip digital counter; as the ramp voltage decreases, the count value decreases. The single-slope conversion works by latching the count value at which the ramp voltage crosses the voltage generated by the image charge. The latch used in the chip described here is a CCD latch; the latch is transparent to the count input until the ramp voltage is lower than the image voltage, after which the latch holds the last digital data stored before the crossover.

The CCD latch was chosen for its compactness and simplicity of data readout; an array of standard digital latches would work equally well but would require significantly more area and a multiplexing scheme for data output. In the $2\mu m$ Orbit n-well process implementation of the interline imager with on-chip A/D conversion, the CCD latch area is $40 \times 47\mu m^2$, including all gates required for data readout. Each set of 8 latches associated with a given image row, then, measured only $320 \times 47\mu m^2$.

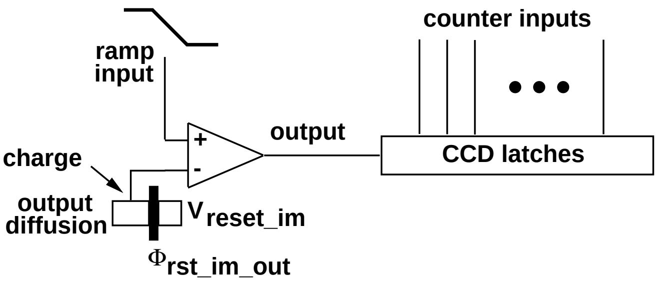

Figure 4: Single-slope A/D converter: charge sink, comparator, and CCD latches.

The CCD latch and digital readout structure is shown in detail in figure 5. As shown in the diagram, the counter inputs are connected to diodes which are adjacent to a vertically aligned CCD shift register. Throughout the time the ramp is descending, the voltage on the storage gates adjacent to each diode (labeled 'st1' in the figure) is kept high, maintaining a potential well under that gate. As long as the comparator output is high, the vertical spurs connected to the comparator output line ensure that no potential barrier exists between the diode and the adjacent storage gate. While the comparator is high, then, if the diode level is high, charge flows from beneath the storage gate to the diode, resulting in an empty charge well under the storage gate. If the diode level is low, however, charge flows from the diode to the storage gate, resulting in a filled charge well under the storage gate.

When the comparator voltage switches from a high to a low value, a potential barrier is established between the diodes and the adjacent storage gates, meaning that any further changes in the voltage input to the diodes have no effect on the charge level in the adjacent storage gates. In effect, then, when a particular comparator output changes from high to low, the count value corresponding to the analog level at which the change occurred is latched in that row. The form in which the data is latched is the pattern of full and empty wells in the set of 'st1' gates in that row. A full well represents a zero; an empty well represents a one.

The ramp voltage at which a given comparator changes state will be the voltage of the imaging CCD output node to which that comparator is connected. As described above, this analog voltage, by virtue of the synchronization of the count and the ramp, is encoded digitally in the value of the count when the state change occurs. The count value at the time the comparator output changes from high to low is latched in the digital output CCD for the remainder of the traversal of the ramp over its range. Once the ramp reaches its final voltage, the digital output CCD shift register is clocked, moving the charge packets in the vertically aligned digital shift registers toward the 8 digital output comparators (one digital comparator per bit). The role of these comparators is to convert the presence or absence of a digital charge packet to digital output voltage levels. If charge is present, the output voltage is high, else the

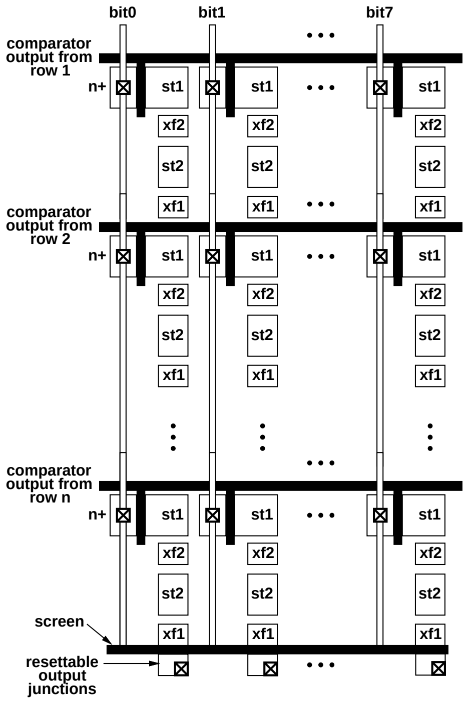

Figure 5: Schematic of the A/D, digital data transfer, and digital output subsystem.

output voltage is low. Each of these digital comparators has one input connected to the charge sink for the digital output CCD and the other input connected to a fixed voltage chosen so that it discriminates the voltage generated by a full digital charge well from that generated by an empty digital charge well.

Once the digital readout is complete, the next column of image data is shifted onto the imager CCD output node/comparator input and the readout process is repeated. Once the whole image has been transferred and converted to a digital format, the process is ready to be repeated for the acquisition of the next frame. The final output of the chip is a stream of 8 bit digital voltage data, where each 8 bit element of the stream is a digital representation of the light level at a single pixel in the imaging array.

4 Test Apparatus

In order to test the CCD interline imaging array with on-chip A/D conversion, it was necessary to generate a number of input control signals. Included among these signals are CCD clock levels for each CCD shift register, reset signals and levels for the photodiodes and CCD output junctions, a transfer signal to shift image charge into the image CCD shift register, a comparator bias level, a dc level for the digital output comparator, and an input ramp synchronized to an input count. Note that it is not difficult to implement circuitry which will generate all of these signals on a single chip; in the prototype circuit, we focused on the core of the imaging and conversion subcircuits.

In order to generate the control signals detailed above as well as acquire image data, we use a word generator coupled with a 20MHz 80386-based personal computer with a standard digital I/O board. We also use a set of external inverters and a set of pulse generators to perform needed level shifting. Because the computer-generated clock does not run fast enough to acquire valid image data, a small memory is used to cache the digital output from the custom chip; the computer reads data from the cache in order to display output images.

In this prototype, testability of the primary elements of the array and converter was optimized. The single-slope, CCD latch-based A/D converter would have been far less complex to control if a counter and ramp generator (an integrator) had been directly included on-chip. Similarly, integrating internal level shift and clock drive circuitry to run all of the CCD subcircuits would have significantly reduced external control requirements. In this first design, however, we wanted maximum access to the core CCD subcircuits. In future designs, we will simplify testing requirements and enhance applicability by focusing on the inclusion of control and bias circuitry on-chip.

5 Results

The imaging chip which was fabricated features a 28×39 interline imaging array as well as a 6-8 bit A/D converter. In this section, we will present A/D converter data and sample imaging array outputs from the test chip.

5.1 A/D Conversion

The test chip, as described above, includes a set of parallel, single-slope A/D converters. It is possible to isolate this subcircuit from the imaging part of the chip and study it directly. In order to achieve this isolation, we must control both the positive and the negative input of each image output comparator. The positive inputs, which receive ramp input, are connected directly to an output pin. The negative inputs are connected to the output junctions of each image transfer CCD. Each of these junctions must be reset before each new charge packet arrives, thus each is connected to a reset voltage level node through a reset gate. Each reset gate and reset level are controlled, respectively, by single, externally supplied signals. If we hold the reset signal high, the reset level is connected to the image output junctions and thus to each negative comparator input. Thus, we have control over both the positive and the negative comparator inputs in the single slope A/D converter.

In order to study the single slope, CCD/CMOS A/D converter, we fed a ramp signal synchronized with a six bit count to each positive comparator input, and fed a set dc levels to the negative comparator input, measuring the digital output as a function of the changing input levels. The response of 15 of the 39 parallel converters is shown in figure 6. Some of the converters (not shown) had problems with major bit transitions; these problems can be solved by using a Gray code instead of a standard binary code as counter input. Our test setup did not allow clean measurement of the seventh bit of the converter; due to a fabrication problem, the counter input connected to the converter's eighth bit was shorted. Note that brighter image pixels yield more image charge, hence lower output voltages as the analog input to the A/D converter; bright spots should correspond to larger digital output values. We achieve this correspondence by inverting the slope of the converter output.

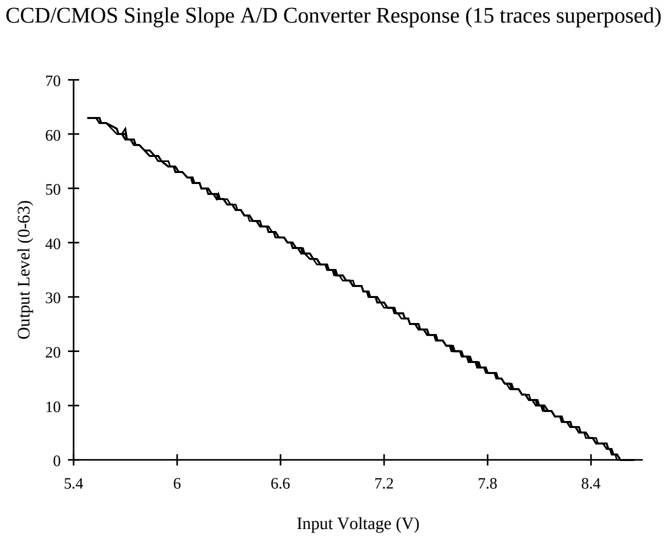

Figure 6: A/D converter response.

5.2 Image Output

Figures 7 and 8 show a collection of image pairs representing raw and smoothed output from the imaging array. In each pair, the lefthand image is an example of raw, 25×28 pixel image data from the chip. These images are corrupted by noise which arises from a number of sources, including clock jitter, bad pixels, and A/D converter non-uniformity. Because the array was fabricated in a process not optimized for CCDs and because the CCDs are all surface channel devices, the presence of relatively high noise levels in the pixels themselves is not surprising. The primitive nature of the test setup also contributed significantly to noise in the output; the 80386-based personal computer used to control the overall clocking process for the chip was especially problematic. Furthermore, the chip which was tested is a prototype and has prototype problems, including, for example, insufficient light shielding in some spots on the chip.

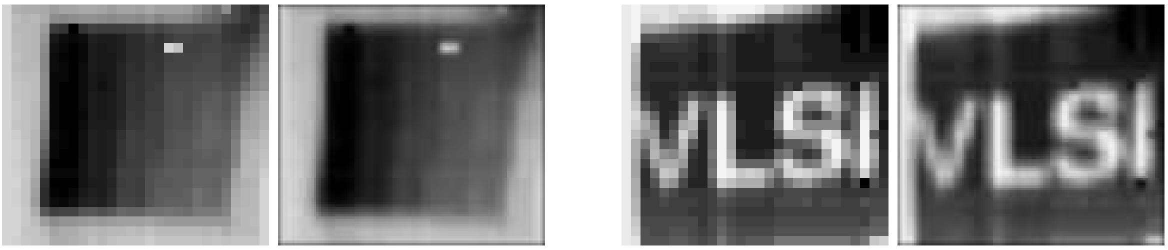

Figure 7: Original and smoothed imaging array output pairs: gray scale bars and white on black text. The original image dimensions are 25×28 and the resolution is 6 bits.

The righthand image in each image pair in figures 7 and 8 represents a smoothed version of the associated lefthand, raw image. The smoothing was accomplished by applying a gaussian filter to the raw image. We present these smoothed images in order to remove the pixel quantization artifacts from the image taken as a whole. Because this chip was implemented through MOSIS as a tinychip ($2.25mm \times 2.22mm$), the array size is necessarily quite small and each pixel stands out in the original images. The smoothing

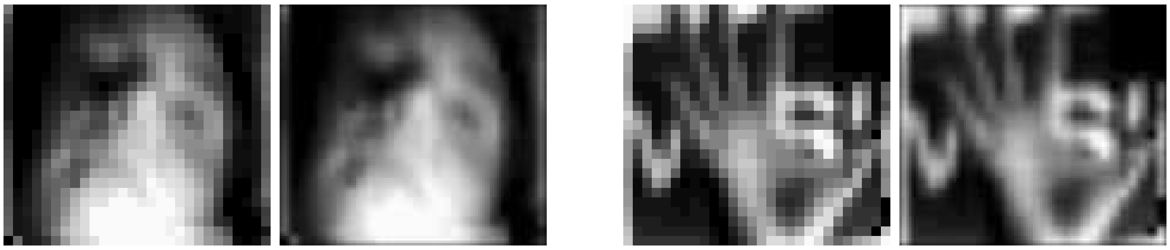

Figure 8: Original and smoothed imaging array output pairs: a face and a hand in front of white on black text. The original image dimensions are 25×28 and the resolution is 6 bits.

gives the effect of a larger implementation in which, of course, the boundaries of individual pixels would not be noticeable.

6 Discussion and Conclusions

In this paper, we describe a CCD interline imager integrated with a set of parallel, single-slope A/D converters. We present A/D converter and whole imager output from devices fabricated through MOSIS. This chip is the first step toward a wholly integrated, single-chip camera with digital output. The price of the added functionality (provided by the A/D converter) is the space required by the conversion circuitry and the extra time in each image acquisition cycle required to perform the conversion.

The area cost of the A/D converter scales with the product of the number of image rows and the number of bits in the conversion. For a $1cm \times 1cm$ design implemented in a $2\mu m$ process, 8-bit A/D conversion should consume approximately 5% of the total chip area. For larger imaging arrays and also for smaller values of λ, the A/D converter area as a percentage of total chip area will be further reduced. Small additional area costs will be incurred by adding control, clocking, and bias signal generating circuitry to the imaging array with the A/D converter structure.

The time cost of the A/D conversion is, effectively, the product of the ramp/counter time and the number of columns in the image. For an 8-bit converter, 256 clock cycles are required to run the counter from its maximum to its minimum value. For a 128×128 imaging array, the imager with A/D conversion requires a factor of 1.5 more time than a similar imager without A/D conversion. Each additional bit of accuracy doubles the time cost of the conversion process. The ultimate limitation on the number of bits which is practical for this conversion technique, however, is probably not the time cost of the operation; instead, variation in both comparator offset voltages and in the capacitance of the image charge output nodes will be critical.

There are a number of ways to improve and enhance the prototype CCD interline imaging array with on-chip A/D conversion presented in this paper. As mentioned earlier, integration of control, clocking, and bias circuitry would yield a compact, easy to operate imager with digital output, potentially requiring only power, ground, a master clock, and a finite state machine to provide the required overall signal pattern. By implementing the design using a true CCD process with buried channel devices, the performance of both the image and digital transfer CCDs would be improved. Given the proof of concept demonstration provided by the prototype chip described here, implementing an array with practical dimensions also makes sense.

Finally, for larger arrays it makes sense to build, on each chip, four parallel sets of A/D converters of the type described above. The converters would be placed in two columns, one on either side of the imaging array, with two converters in each column. The top converter in the righthand column would transfer digital data up and would serve the upper righthand quarter of the imaging array, the bottom converter in the righthand column would transfer digital data down and would serve the lower righthand quarter of the imaging array; the lefthand A/D converters would process image charge moving from right to left, with the top converter serving the upper lefthand image quarter and the bottom converter serving the lower lefthand image quarter.

In this paper, we describe an architecture for an interline imaging array with on-chip A/D conversion as well as a particular implementation of that architecture. The test results we present from that implementation show that the chip functions as a small-scale imager, yielding digital output corresponding to input light intensity. By implementing the improvements suggested above, we hope to expand on our work to date, ultimately developing a practical, single-chip imager with digital output.

7 Acknowledgements

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References

[1] K. Chen, M. Afhahi, P. E. Danielsson, and C. Svensson, "PASIC: A Processor-A/D Converter-Sensor Integrated Circuit," in **Proceedings of the International Symposium on Circuits and Systems**, pp. 1705-1708, May, 1990.

[2] S. Soclof, Applications of Analog Integrated Circuits, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1985, pp. 515-526.

[3] D. F. Barbe, "Imaging Devices Using the Charge-Coupled Concept," in **Proceedings of the IEEE**, Volume 63, Number 1, January, 1975, pp. 38-67.